Linearity Enhancement Analysis of Breakdown Voltage Doubler and Demonstration in 60 GBd SiGe BiCMOS Driver

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***Abstract*—In this paper, we prove theoretically and experimentally the enhanced linearity behaviour of the BVD topology compared to the more well-known cascode topology in terms of THD, 1dBCP and R_{LM}. We present the nonlinear algebraic analysis and simulations of the topology, along with the measurements of a high-speed, large output swing, linear, four channel optical modulator driver IC using that topology. The realised driver has an electrical 3 dB-bandwidth of 30 GHz and a differential output swing of 2.5 Vppd with a power consumption of 480 mW per channel. It achieves an R_{LM} of 0.98, THD of < 2 % and output referred 1dBCP of 11.4 dBm.**

***Index Terms*—Breakdown Voltage Doubler, optical modulator driver, nonlinearity analysis, SiGe BiCMOS, high-speed Integrated Circuits**

I. Introduction

In the pursuit of ever increasing data rates in optical communication links, linearity has become a defining aspect for the electronic and photonic transceiver circuits, driven by the adoption of multi-level modulation formats like high-order Pulse Amplitude Modulation (PAM) and Quadrature Amplitude Modulation (QAM). During the design of a linear high-swing modulator driver IC based on a Breakdown Voltage Doubler (BVD) [1, 2], an improvement in the most relevant linearity measures, such as Total Harmonic Distortion (THD), 1dB Compression Point (1dBCP) and Level Separation Mismatch Ratio (R_{LM}) [3] was observed with respect to a conventional cascode driver topology. In this paper, the linearity improvement is demonstrated analytically and further illustrated through simulations and measurements.

II. Algebraic Analysis

Originally, the BVD was designed to divide the output voltage swing over both transistors in a cascode configuration, where normally, the cascode transistor would take the majority of the voltage swing. By dividing the swing over both transistors, breakdown is only reached for higher output voltage swings. However, the degree of linearity associated with the BVD topology has not been extensively explored in existing literature.

In our study, we initiated an algebraic analysis of the BVD circuit, as depicted in Fig. 1b (compared to the conventional cascode circuit in Fig. 1a). Our focus was on the signal and nonlinearity contributions of the circuit specifically to the transistors Q_3-Q_4, where the key difference emerges. Differential pair Q_5-Q_6 was assumed to contribute a sinusoidal voltage at the base of Q_3-Q_4, while differential pair Q_1-Q_2 contributes a sinusoidal current at the emitter of Q_3-Q_4. For the following analysis, the equivalent half circuit pictured in Fig. 1c was used. Consider the output voltage of this circuit, v_{out}, which can be written as:

$$v_{out} = V_C = V_{DD} - R_L I_C \tag{1}$$

with V_{DD} the supply voltage and I_C the collector current, according to the Ebers-Moll equations [4]:

$$I_C = I_S\left[\left(\exp\left(\frac{V_{BE}}{V_T}\right) - \exp\left(\frac{V_{BC}}{V_T}\right)\right) - \frac{1}{\beta_R}\left(\exp\left(\frac{V_{BC}}{V_T}\right) - 1\right)\right] \tag{2}$$

where I_S is the reverse saturation current, V_T the thermal voltage, β_R the reverse current gain, V_{BE} the base-emitter voltage and V_{BC} the base-collector voltage. Except for V_E, V_C and I_C, all variables in Eqs. (1) and (2) are known. The Ebers-Moll equation for the emitter current I_E can be used to determine V_E, with β_F the forward current gain:

$$I_E = I_S\left[\left(\exp\left(\frac{V_{BE}}{V_T}\right) - \exp\left(\frac{V_{BC}}{V_T}\right)\right) + \frac{1}{\beta_F}\left(\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right)\right] \tag{3}$$

To simplify the expression for V_E, $\exp\left(\frac{V_{BC}}{V_T}\right)$ can be approximated using a first order Taylor expansion, where $V_{BC,Q}$ is the quiescent component and $v_{bc,s}$ the signal component of the base-collector voltage, and $\xi = \exp\left(\frac{V_{BC,Q}}{V_T}\right)$:

$$\exp\left(\frac{V_{BC}}{V_T}\right) = \xi\left(1 + \frac{v_{bc,s}}{V_T}\right) \tag{4}$$

V_E can then be written as:

$$V_E = -\ln\left(\frac{V_T(\beta_F I_E + I_S) + \xi\beta_F I_S(v_{bc,s} + V_T)}{V_T I_S(\beta_F + 1)}\right)V_T + V_B \tag{5}$$

Now, V_B and I_E are split up in their quiescent and signal components as well, according to Eqs. (6) and (7). Both signal components originated from the same source, v_{in}, which is assumed to be sinusoidal, but the voltage at the base of Q_3 has received a sign inversion from differential pair Q_5-Q_6, while the current at the emitter has not, so they appear with 180° phase difference. Both signal components are represented by I_{sig} and V_{sig}.

$$I_E = I_{E,Q} + i_{e,s} = I_{E,Q} + I_{sig}\sin(\omega t) \tag{6}$$

$$V_B = V_{B,Q} + v_{b,s} = V_{B,Q} - V_{sig}\sin(\omega t) \tag{7}$$

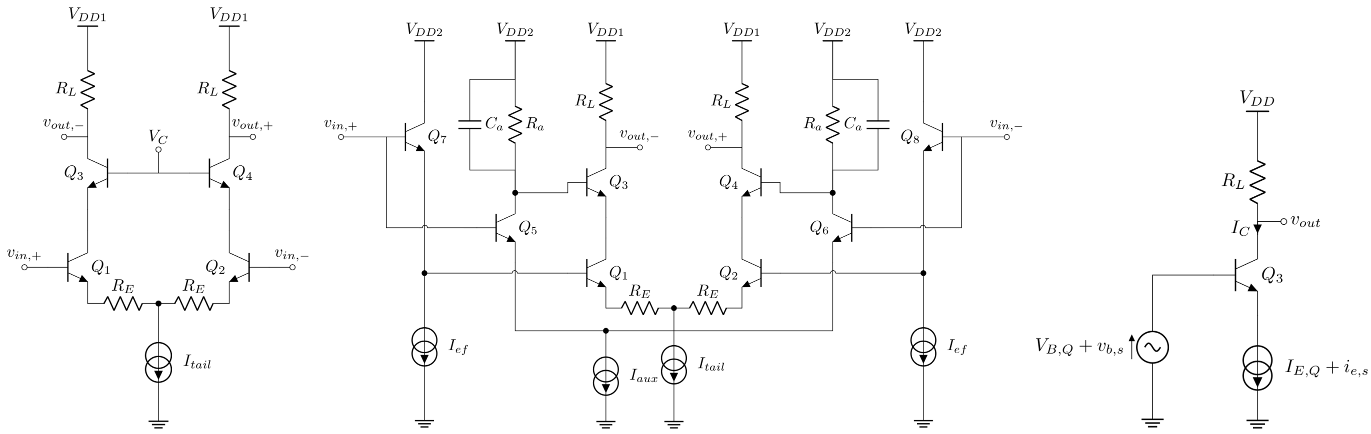
Now, the natural logarithm in Eq. (5) is approximated by its Taylor series:

$$\ln(1+x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \frac{x^4}{4} + \ldots \tag{8}$$

It is clear that these higher order terms will give rise to unwanted harmonics. When a third order approximation is considered, the coefficient for $\sin^3(\omega t)$ becomes:

$$\lambda_3 = \frac{\left(V_T I_{sig} - \xi I_S V_{sig}\right)^3 \beta_F^3}{3V_T^3 I_S^3(\beta_F + 1)^3} \tag{9}$$

Now, Eqs. (1) and (2) form a system of two equations in two unknowns, I_C and V_C. The system can be solved using the third order approximation for the natural logarithm function in Eq. (5). The $\exp\left(\frac{V_{BE}}{V_T}\right)$ term in Eq. (2) can be approximated using a similar Taylor expansion of equal order, in order to preserve the harmonic mixing that will occur due to the exponential relationship between V_{BE} and I_C.
Therefore, when a third order approximation is used, v_{out} has up to ninth order terms, due to third order terms in V_E mixing with the third



(a) (b) (c)

Fig. 1. Simplified schematics of a conventional cascode with emitter degeneration (a) BVD with emitter degeneration (b) and signal contributions to analyse the behaviour of Q_3 (c)

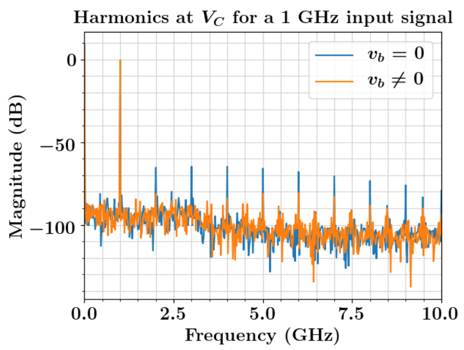


Fig. 2. Simulated harmonics when a 1 GHz tone is supplied at both inputs of Q3 (BVD operation, orange, THD = 0.043 %) and only at the emitter of Q3 (cascode operation, blue, THD = 0.137 %)

order approximation for I_C. However, all terms higher than second order are proportional to $\xi I_S V_{sig} - I_{sig} V_T$, similar to Eq. (9). Most of the second order terms are proportional to this quantity as well, except for a term proportional to V_{sig}^2 and a term proportional to V_{sig}. Since this difference appears in all harmonics, they will cancel out when $\xi I_S V_{sig} = I_{sig} V_T$ and be reduced significantly when equality is not exactly achieved due to process or temperature variations. The additional second order harmonic terms will be reduced by using a differential topology.

Contrasting this, when the cascode architecture of Fig. 1a is used, there is no voltage signal present at the base of Q_3, which effectively means that $V_{sig} = 0$ and no suppression of the harmonics is present.

Since a few approximations were made to conclude this result, the Cadence Spectre simulator was used to obtain the same conclusions without assumptions, which can be found in Fig. 2. A voltage signal of 280 mVpp and a current signal of 64 mApp were presented to Q_3's base and emitter respectively. The amplitudes of these signals, as well as the termination resistor R_L match those used in the driver design of Section IV. It is clear to see that all harmonics are repressed at least 10 dB, and the third harmonic is eliminated completely.

III. Simulations

For the following numerical analysis, both the cascode and BVD architectures were simulated with the Spectre simulator in Cadence using the foundry models for all Bipolar Junction Transistors (BJTs). For a fair comparison, the supply voltages, bias currents, degeneration resistors and $V_{CE,Q}$ and $V_{BE,Q}$ voltages were kept identical. However, under these conditions, the BVD architecture consumes about 19 % more power than the cascode architecture, amounting to 374 mW and 316 mW respectively. By either decreasing the tail current of the BVD or increasing the tail current of the cascode architecture, we can compensate for this. The results of all four cases are summarised in Fig. 3.

From Figs. 3a and 3b, we can see that when foundry models are used, the linearity as defined by THD and R_{LM} is very similar up to 2 Vppd output swing, and then the BVD begins to outclass the cascode. Figs. 3c and 3d show both the input and output referred 1dBCP. It is clear that for similar DC power consumption, the BVD topology not

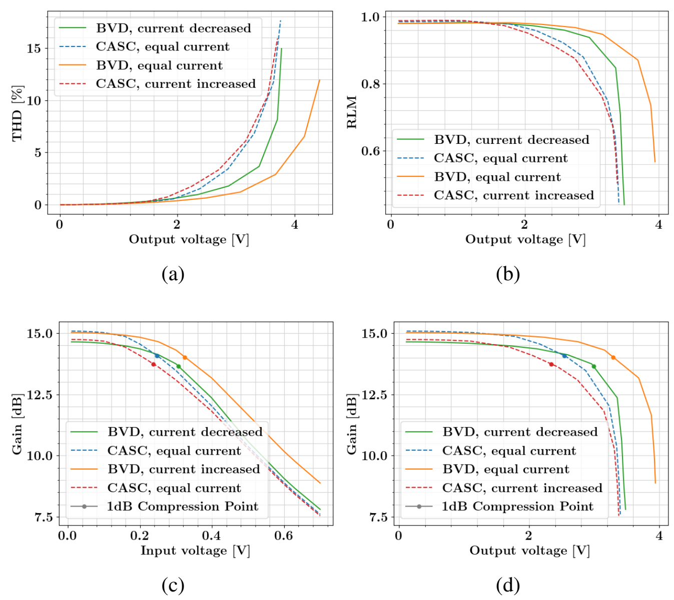


Fig. 3. Simulation results for vendor models (a) THD (b) R_{LM} (c) Input referred 1dBCP (d) Output referred 1dBCP. Cascode topology (blue), BVD topology (yellow), cascode with increased current (red), BVD with decreased current (green)

only outperforms the cascode topology in linearity, but additionally it also achieves a higher gain and output swing.

IV. Measurements

The BVD circuit was integrated in the output stage of a high-swing (up to 2.5 Vpp) linear driver Integrated Circuit (IC), whose output is optimized to interface with an Electro-Absorption Modulator (EAM), which presents a capacitive load of 300 fF. In order to achieve 30 GHz bandwidth, both 150 pH shunt peaking inductors were added in series with R_L, and R_L was chosen to be 30 Ω, instead of 50 Ω, to diminish the RC-product of termination resistor and EAM capacitance. The degeneration resitor R_E was sized to be 2 Ω. Fig. 4 shows the die micrograph of the realised four-channel linear differential driver IC. It was fabricated in a 130 nm SiGe BiCMOS process. It measures 1.21 mm by 2.71 mm with a channel pitch of 375 µm. All low speed Serial Peripheral Interface (SPI) and DC pads were wirebonded to a Printed Circuit Board (PCB). During all measurements, the high speed input and output pads were connected using RF probes. The supply voltage for the main branch of the BVD output stage was 4 V, while the input buffer, Variable Gain Amplifier (VGA) and all other bias blocks had a supply of 2.5 V. The total power consumption of the chip during the measurements was 1.92 W, which corresponds to 480 mW per channel. Before eye diagrams were captured on the sampling scope, the frequency dependent losses internal to the Arbitrary Waveform Generator (AWG), the connecting cables and the probes were calibrated out using Keysight's IQtools software.

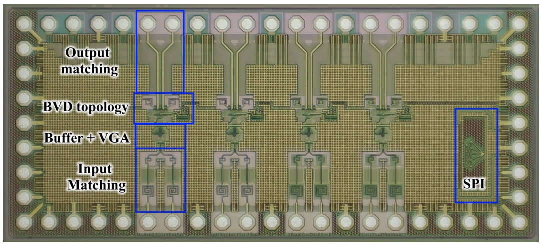
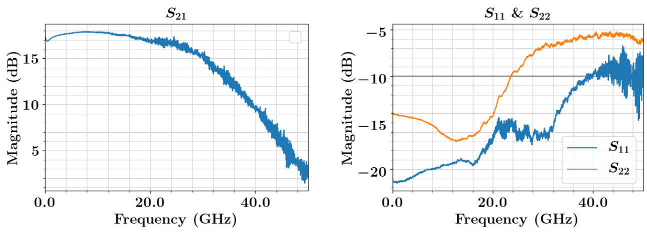


Fig. 4. Micrograph of the proposed driver IC with BVD output stage

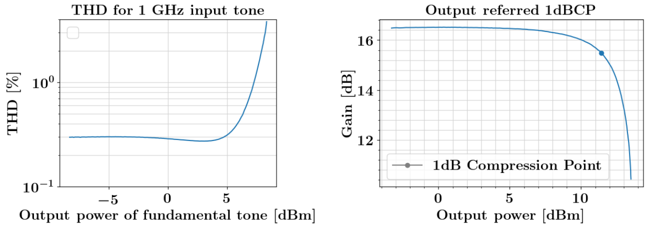
A. S-Parameter Measurements

The presented S-parameter measurements were conducted using a Keysight N5247B PNA-X. The S-parameters were measured from 10 MHz to 50 GHz using an IF bandwidth of 10 kHz and an input power of −5 dBm. As shown in Fig. 5b, the differential S_{11} is lower than −10 dB up to 35 GHz, whereas the differential S_{22} rises above −10 dB from 25 GHz, due to the inherent mismatch between the output impedance of the driver chip (30 Ω plus peaking, to optimize the bandwidth when driving an EAM) and the 50 Ω reference impedance of the S-parameter measurement. As seen in Fig. 5a, the DC gain is 17 dB and the electrical 3 dB-bandwidth is 30 GHz. After characterising the S-parameters, a power sweep was performed to gain insight in the (input referred) 1dBCP of the driver IC, the result of which can be seen in Fig. 6b. The 1dBCP is measured at −3.4 dBm for a 10 GHz input. The THD was also measured by looking at up to the eighth harmonic of a 1 GHz tone. The dependency of the THD as function of output power is visualised in Fig. 6a. It only reaches 2 % at an output power of 7.9 dBm. This would correspond to a peak-to-peak voltage of 1.6 V when both driver and load would be 50 Ω, but since there is a mismatch between the internal 30 Ω termination and the external 50 Ω measurement impedance, the voltage experienced by a capacitive modulator such as an EAM will be closer to 2.5 Vppd.



(a) (b)

Fig. 5. Measured S-parameters (a) S_{21} for different VGA settings (b) S_{11} and S_{22}



(a) (b)

Fig. 6. Measured linearity results: (a) THD for a 1 GHz input tone (b) output referred 1dBCP

B. Time Domain Measurements

A PRBS-15 input signal was generated using a 92 GSa/s, 32 GHz analog bandwidth, Keysight AWG (M8196A) and applied to the driver input high speed bond pads using RF cables and GSSG RF probes. Analogously, the output signal of the IC was connected to Keysight 86118A 70 GHz remote sampling heads installed in a DCA-X sampling scope with similar RF probes and cables.
The eye diagram for a 60 GBd PAM4 signal can be seen in Fig. 7. In the oscilloscope, a 5-tap Feed Forward Equaliser (FFE) is used to remove linear distortion due to Inter Symbol Interference (ISI). The eye diagram has an amplitude of 1 Vppd and an R_{LM} of 0.98. A similar argument as in Section IV-A can be made here as well, because of the internal 30 Ω termination, an EAM will experience a larger signal swing. Additionally, in the eye diagram of Fig. 7, there were some cables not corrected for. Combining these two facts again indicates an output swing of around 2.5 Vppd.

To have an idea of the relative power penalty the driver would

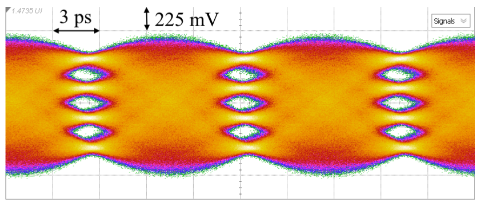


Fig. 7. Eye diagram for 60 GBd PAM4, after 5-tap FFE.

introduce in a real-world system, the Transmitter Dispersion Eye Closure Quatenary (TDECQ) [12] is measured for different baud rates. TDECQ quantifies the power penalty related to eye deterioration. A standard target Symbol Error Rate (SER) of 4.8×10^{-4} was used. The result is shown in Fig. 8b, where it is clear that TDECQ stays below

TABLE I

COMPARISON TO STATE-OF-THE-ART LINEAR LUMPED DIFFERENTIAL DRIVERS

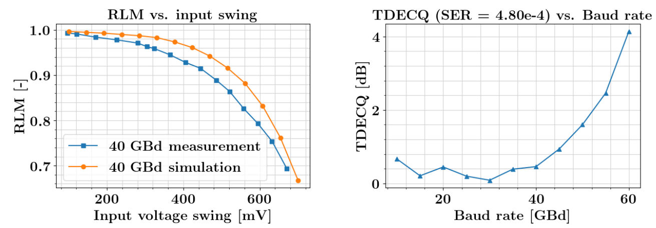
	This work	[5]	[6]	[7]	[8]	[9]	[10]	[11]
Technology	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	700 nm InP DHBT	90 nm SiGe BiCMOS	130 nm SiGe BiCMOS	700 nm InP DHBT	700 nm InP DHBT	130 nm SiGe BiCMOS
Architecture	BVD	BVD	cascode	SEFPP [a]	BVD	cascode	cascode	BVD
Data Rate (GBd)	60 (PAM4) / 40 (PAM8)	45 (PAM4)	50 (PAM4)	56 (PAM4)	80 (PAM4)	80 (PAM4)	90 (PAM4)	69 (PAM4)
Modulator Impedance	50 Ω / 300 fF	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω
Output Swing (Vpp)	1.6 / 2.5 [b]	6.5	4.9	3.6	4	3	3	2.4
Power consumption (mW)	480	670	1200	900	990	740	670	1000
Efficiency (pJ/bit)	4	7.44	12	8.05	6.18	4.62	3.72	7.14
OR1dBCP (dBm)	11.4	-	-	-	-	9	9.1	-
THD (%)	< 2	1	5	2.61	-	-	2.7	3.6
R_{LM}	0.98	-	-	-	0.913	-	-	-

[a] Single Emitter Follower Push Pull [b] depending on modulator impedance

3 dB up to 56 GBd.

In order to compare the PAM4 performance to a simulation, the R_{LM} was measured for different input voltages at 40 GBd, shown in Fig. 8a. Clearly, the R_{LM} has a similar behaviour as the simulated values.

To conclude the time domain measurements, also higher order PAM



(a) (b)

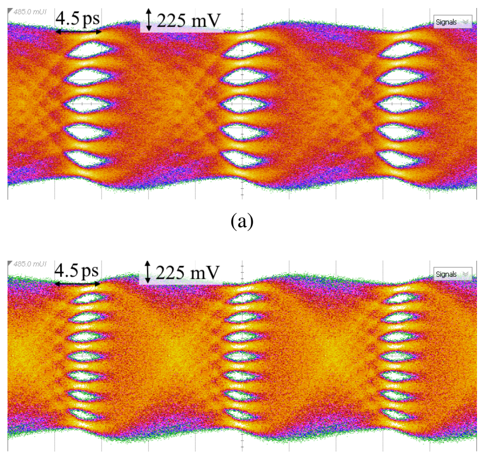
Fig. 8. R_{LM} as function of input swing at 40 GBd for measurement and simulation (a) and TDECQ measurements as function of symbol rate (b)

formats were used as input signals. Both PAM6 and PAM8 modulation formats did not experience compression. The eye diagrams for a 40 GBd input signal can be seen in Figs. 9a and 9b. A slightly lower baudrate was used in these higher order measurements because ISI becomes more pronounced in higher order modulations.

C. Comparison to State-of-the-Art

Table I summarizes the state of the art of highly linear lumped differential modulator drivers. The proposed driver shows the lowest power consumption while still having good linearity specifications.To the author's knowledge, this driver is the most power-efficient lumped linear driver among all SiGe BiCMOS implementations.

From the table, it is also clear that drivers designed with a BVD topology tend to have better linearity than the cascode topologies: [6, 10], both cascode topologies, reported a higher THD than this work and [5], both BVD topologies. Although all reported PAM4 eye diagrams seem to have little level separation, a reliable estimate on the R_{LM} values cannot be made from the graphs in those papers. Only few 1dBCP have been reported, but the ones in [9, 10] use a cascoded topology and report a lower 1dBCP. All of these ascertainments support our theoretical analysis results on linearity enhancement using a BVD topology.



(a) (b)

Fig. 9. 40 GBd higher order PAM, with 5 taps of FFE . (a) PAM6 (b) PAM8

V. CONCLUSION

In this paper, we managed to theoretically demonstrate that the BVD architecture enhances the linearity of the circuit in which it is used. Additionally, simulations using vendor models were provided that support this hypothesis in the linearity measures THD, R_{LM} and 1dBCP. Lastly a prototype IC based on the BVD topology was presented with a power consumption of 480 mW which can drive an EAM at 60 GBd PAM4 with an output swing of 2.5 Vppd and an R_{LM} of 0.98 or at 40 GBd PAM8, which positions it among the most linear drivers in the state of the art.

VI. ACKNOWLEDGEMENT

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