Epitaxial SiGe/Si multi-stacks: from stacked nano-sheet to fork-sheet and CFET devices

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The scaling evolution from stacked nano-sheet devices to fork-sheet devices and CFET architectures went together with increased complexities of the epitaxial growth schemes. This is valid for both the Si/SiGe multi-layers which define the thickness of the nano-sheet channels as well as the vertical distance between individual nano-sheets and also for the epitaxially grown source/drain (SD) layers which require a continuous increase in active doping concentration and a reduction in thermal budget without compromising material quality.

Fork-sheet transistors are lateral nano-sheet devices with a forked gate structure [1,2]. The physical separation of n- and p-devices by a dielectric wall enables device scaling and, consequently, sheet width maximization within the limited footprint of low-track-height standard cells. Bottom dielectric isolation has been proposed to circumvent the junction isolation trade-off between punch-through suppression on the one hand and junction leakage and capacitance on the other hand [3]. A typical fabrication scheme includes the challenging epitaxial growth of fully strained Si/$Si_{1-y}Ge_y$/multi-{$Si_{1-x}Ge_x$/Si} epi stacks (y>x) where the bottom Ge-rich $Si_{1-y}Ge_y$ layer is later replaced by a SiN/SiCO isolation [4,5].

In the CFET architecture, n- and p-MOS devices are placed on top of each other, thus completely removing the area consumption by the n-p spacing. This allows for further maximizing the effective channel width and, hence, the drive current [6-9]. The architecture can be fabricated following either a monolithic or a sequential approach. In the first option, n- and p-MOS transistors are built on the same wafer, while the sequential fabrication flow is based on wafer-to-wafer bonding techniques. The strengths and challenges of both approaches are discussed in [9]. In the monolithic approach, device fabrication starts with the epitaxial growth of an even more complicated Si/SiGe multi-stack with two different Ge concentrations (Fig. 1) [10], and where Ge-rich $Si_{1-y}Ge_y$ layers are later replaced by isolating dielectrics [9]. Owing to the very small dimensions (e.g., sub-10 nm nano-sheet channel width), high etching selectivity of the $Si_{1-y}Ge_y$ layers towards both $Si_{1-x}Ge_x$ and Si, and excellent process controls are mandatory. This sets stringent requirements on the epitaxial layer stacks (thicknesses and composition control, sharpness of interfaces, and absence of strain relaxation) [4,5,10,11] as well as on the $Si_{1-y}Ge_y$ etch process (high selectivity, limited consumption of $Si_{1-x}Ge_x$ and Si) [11-14].

To alleviate scaling-related contact issues in these devices, high performance metal / SD junctions are key [15]. Selective epitaxial growth (SEG) processes yielding heavy active doping are therefore required (Fig. 2), in addition to introducing innovative contact materials and designs [16-18]. The resulting electrical performance is, however, restricted by doping solubility limits and loading effects (impact of substrate patterning) inherent to scaling. Those must be circumvented to enable the upcoming generations of components. Moreover, novel

device architectures add stringent constraints regarding pre-epi cleaning strategies, thermal budgets, and stability.

This work describes the material requirements of the different layers and the progress made on the associated epitaxial growth techniques.

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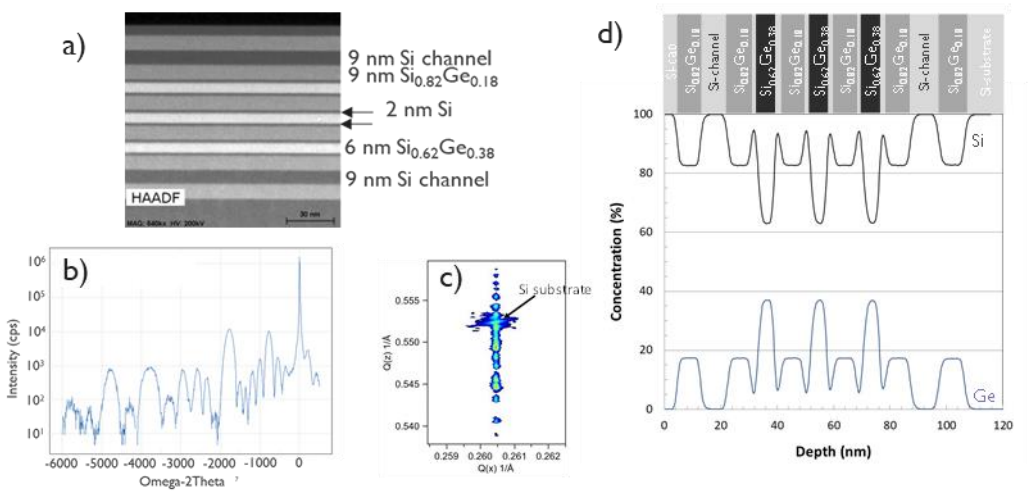

Fig. 1 a) HAADF STEM of a SiGe/Si multi-stack used for CFET devices, b) XRD ω-2θ scan acquired around the Si 004 Bragg reflection, c) XRD-RSM around the Si 113 Bragg reflection, and d) Ge and Si Extremely Low Impact Energy (EXLIE)-SIMS profiles confirming the sharp interfaces as extracted from integrated STEM contrast analysis.

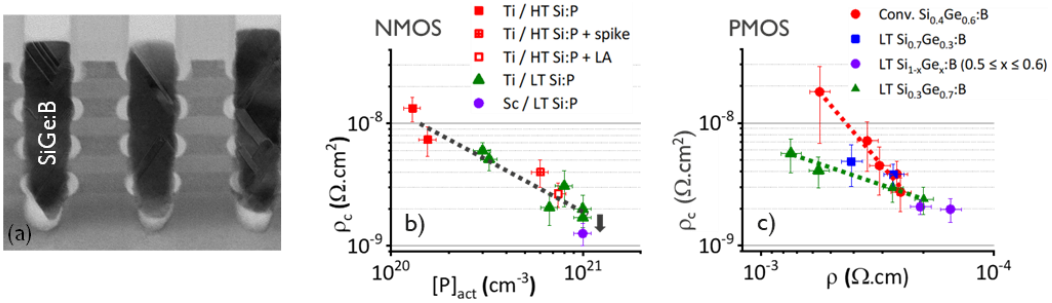

Fig. 2 a) X-TEM showing SiGe:B SD grown in 48 nm CPP nano-sheet structure, b and c) comparison of contact resistivities obtained on CTLM structures using conventional and lower temperature (LT) Si:P and SiGe:B processes, respectively [16].