O-band GaAs QD-on-Si integrated optical amplifier realized using micro-transfer printing

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***Abstract*—We present the integration of O-band GaAs QD-on-Si integrated optical amplifiers on an advanced silicon photonics platform using micro-transfer printing. The resulting devices exhibit 6.5 dB on-chip gain at 1292 nm.**

Keywords—Silicon photonics, III-V-on-Si integration, GaAs quantum dots, optical amplifier, micro-transfer printing

I. INTRODUCTION

Silicon photonic (SiPh) integrated circuits offer the ability to create highly miniaturized optical systems on a single chip, thanks to the high index contrast between silicon (Si) and the surrounding silicon dioxide (SiO_2) cladding. By incorporating monolithically integrated germanium on silicon components, SiPh platforms have a wide range of functional capabilities that can be tailored to meet specific application requirements. In recent decades, the rapid development of a variety of components with continually improving performance has made Si PICs readily available in foundries. However, the lack of essential functions, such as optical amplifiers and light sources, has become a significant obstacle to improving the performance of Si PICs while maintaining their small footprints. To address this issue, various approaches have been explored, including flip-chip and pick-and-place-based micro-assembly, (multi-) die-to-wafer bonding, and hetero-epitaxial growth. Among these approaches, micro-transfer printing (μTP) has shown high throughput and potential for low-cost heterogeneous integration of a variety of non-native materials/components on SiPh wafers. μTP allows for the realization of opto-electronic devices and Si PICs separately, leveraging the mature III-V processes and CMOS processes in foundries, similar to flip-chip/pick-and-place assembly. Compared to (multi-) die-to-wafer bonding, μTP requires minimal modification to the well-established Si back-end process flow. Today, complex Si PICs can be manufactured on 200 mm or 300 mm wafers in high-volume and at low cost using well-established CMOS processes.

In this work, we developed a full process flow for the integration of GaAs QD devices on advanced SiPh platforms using μTP. Following this process flow, a large number of GaAs QD SOAs were fabricated in dense arrays on the native substrate and were then undercut by selectively wet etching the AlGaAs sacrificial layer. The pre-fabricated GaAs QD SOAs were picked-up and transfer-printed on to a target SiPh chip with a thin spray-coated divinylsiloxane-bisbenzocyclobutene (DVS-BCB) layer using a polydimethylsiloxane (PDMS) stamp with a single post. Only a few simple processes including DVS-BCB curing, and metal lift-off are required to finalize the fabrication process. The resulting devices exhibit a differential resistance of 3 Ω at the bias current of 130 mA and over 6.5 dB on-chip gain at the wavelength of 1292 nm.

II. MICRO-TRANSFER PRINTING

Micro-transfer printing is a promising approach for heterogeneous integration that relies on an elastomeric PDMS stamp to transfer device coupons from a source wafer onto a target substrate. By controlling the velocity of the stamp in the μTP process, device coupons can be picked up from the source wafer or printed onto the target substrate [1]. A release layer that can be selectively etched should be incorporated between the device layers and the substrate to enable device release. μTP can be performed using a PDMS stamp with a single post, and the devices are picked up and printed onto the target substrate in a one-by-one sequential manner. This process is similar to flip-chip/pick-and-place assembly and ittakes less than one minute to complete one printing cycle, and passive alignment is achieved through alignment marks and pattern recognition process. The throughput of this process can be boosted by using a stamp with an array of posts to manipulate a large number of devices simultaneously. Furthermore, μTP can be fully automated, and state-of-the-art transfer printing tools can achieve alignment accuracy of <1

µm @ 3σ or better [2][3]. More detailed description of µTP is referred to Ref[4].

III. Integration of GaAs QD devices on Si using MTP

Fig.1 shows the complete process flow for the integration of GaAs QD devices on an advanced SiPh platform, e.g. the imec isipp50g platform [5]. The fabrication begins with a GaAs/AlGaAs sacrificial layer removal and a thin SiN layer deposition. The SiN is then patterned through an e-beam lithography process using a thin layer of hydrogen silsesquioxane (HSQ) resist, as shown in Fig.1(a). After that the p-AlGaAs cladding mesa is defined by ICP etching with a gas mixture of BCl_3/N_2 (Fig.1(b)), followed by a PECVD deposition of a thin SiN layer. This SiN layer is used as a hard mask to pattern the QD active region (Fig.1(c)). Then a pair of n-metal contacts are deposited at both sides of the GaAs QD rib waveguide, which is passivated with a thin SiN layer (Fig.1(d)). The SiN layer is also used as a hard mask to define the first coupon mesa by etching through the AlGaAs release layer into the substrate. Then the coupon mesa is covered by thick double-dielectric layer of SiN/SiO_2 (Fig.1(e)). The topography over the top surface of the sample is planarized using a thick layer of BCB and the p-metal contact is deposited after etching back the BCB layer (Fig.1(f)). Then the SiN/SiO_2 encapsulation layer around the first coupon mesa, where the tether structures will be defined, is exposed by RIE etching with a thick photoresist soft mask. As shown in Fig.1(h), The fabrication of GaAs QD SOAs is finalized with the tether definition. Now the sample is ready for release etching, that is carried out by submerging the sample in a 1:1 37% HCl:DI etchant at 15 °C for about 1 hour.

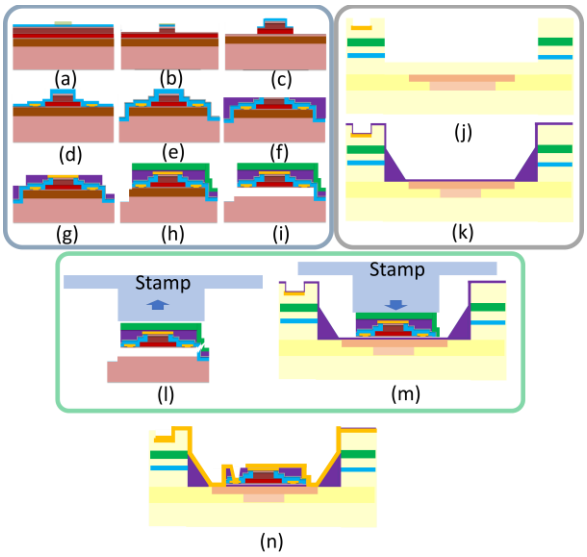

Fig. 1. Process flow for the integration of GaAs QD devices on an advanced SiPh platform through µTP . (a-c) Definition of GaAs QD rib waveguide, (d) n-contact metal deposition and SiN hard mask deposition, (e) the first coupon mesa definition and SiN encapsulation, (f) BCB planarization, (g) the second coupon mesa definition, (h) SiN tether definition, (i) release etch, (j) target SiPh wafer with shallow-etched recesses, (k) back-end removal and DVS-BCB spray coating, (l) pick-up and (m) transfer printing of GaAs device coupon into the recess, (n) DVS-BCB curing and final metallization.

The advanced SiPh platforms consist of a back-end layer stack, therefore an additional back-end opening process is required to expose the local Si device layer to facilitate the integration of III-V components in these platforms. Fig. 1(j) shows the schematic of the imec iSiPP50g platform, where shallow recesses have been defined over the area where the III-V components will be integrated. The residual cladding in the recess is around 2 µm thick and can be easily removed through HF-based wet etching. Prior to the µTP process, a thin adhesive layer of DVS-BCB is spray-coated on the Si substrate (Fig.1(k)), followed by a short soft bake at 150 °C. A set of fiducial markers are respectively patterned on the III-V device coupon and on the Si PICs for the automatic alignment using pattern recognition. After µTP (Fig.1(l)-(m)), only a few simple processes, including DVS-BCB curing and metal lift-off, are needed to finalize the integration. A schematic of the cross section of the resulting transfer-printed GaAs devices with metal contact pads is illustrated in Fig.1(n).

IV. Design and Farbication of GaAs QD-on-Si amplifier

The design of the GaAs QD-on-Si integrated optical amplifier is shown in Fig.2. It consists of a straight GaAs QD/Si hybrid waveguide in the middle and an alignment tolerant III-V/Si taper structures at each side to couple the optical mode from/to the underlying polysilicon (Poly-Si)/Si waveguide, which is followed by a poly-Si/Si taper to further couple the optical mode to a standard O-band Si wire waveguide. As shown in Fig.1(n), a reversed Si rib waveguide with an overall thickness of 380 nm is used in the III-V/Si hybrid waveguide. This waveguide structure is comprised of a 9 µm (width) × 220 nm (thickness) wire waveguide and a 40 µm (width) × 160 nm (thickness) poly-Si slab layer on top. The GaAs QD rib waveguide has a 6.5 um wide QD active region and a 2 µm wide p-cladding mesa. The overall III-V/Si taper structure is 340 µm long, consisting of a 90 µm long rapid taper and a 250 µm slow taper. The widths of the p-cladding mesa, QD waveguide, Si waveguide at the taper tip are ~100 nm, ~500 nm and 2 µm, respectively. Due to the index matching between the poly-Si/Si rib waveguide and the GaAs rib waveguide, no obvious coupling loss or reflection are observed in the simulation for a lateral misalignment of up to 1 µm, in case of a 30 nm thick DVS-BCB bonding layer. Fig.2(b)-(c) depicts the fundamental TE mode propagation through the proposed III-V/Si taper structure.

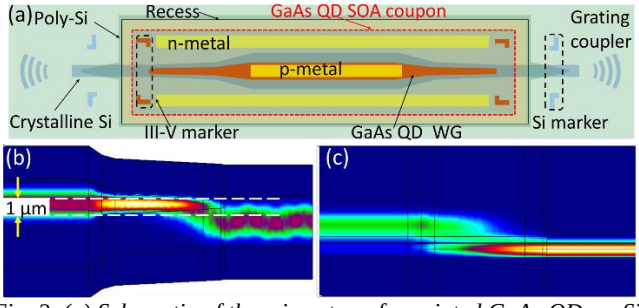

Fig. 2. (a) Schematic of the micro-transfer-printed GaAs QD-on-Si amplifier. (b) The top-view and (c) the side-view of the fundamental TE mode propagating through the III-V/Si taper structure with 1 µm lateral misalignment.

An AlGaAs/GaAs epitaxial structure consisting of a 1 µm thick p-$Al_{0.8}Ga_{0.2}As$ cladding layer, 12 layers of GaAs/InAs QDs and a 350 nm thick n-GaAs contact layer was used in this fabrication. Following the process flow explained in section III, GaAs QD SOAs in dense arrays were fabricated, as the microscope image shows in Fig. 3(a). A lab-scale µTP tool (X-Celeprint µTP-100) was used for the transfer printing and that was carried out at room temperature in the cleanroom

of Ghent university. Given a footprint of 60 µm ×1700 µm of the pre-fabricated GaAs SOA coupons, a PDMS stamp with a single post with comparable dimensions was used. Fig. 3(b) shows the micro-transfer-printed optical amplifiers after final metallization.

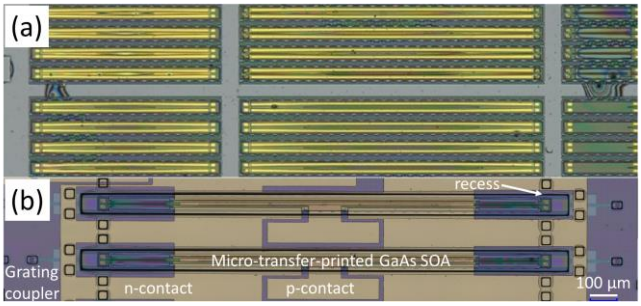

Fig.3 (a) Microscope images of the released GaAs QD SOAs and (b) resulting GaAs QD-on-Si optical amplifiers.

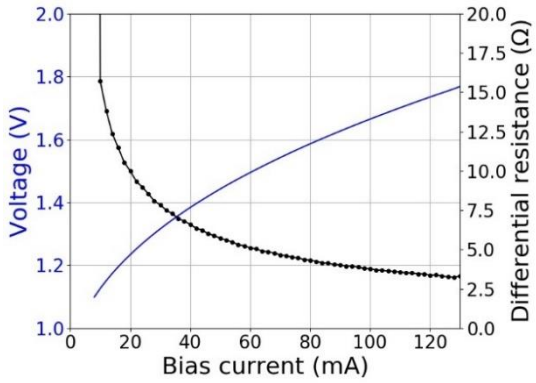

Fig.4 Measured V-I response of a representative device and differential resistance.

V. Performance of the Resulting Devices

The resulting GaAs QD-on-Si integrated optical amplifiers were characterized on a vertical setup where the sample stage was stabilized at 20 °C. A Keithley 2041A current source is used to provide the bias current, which is applied onto the device through a pair of DC probes. Two standard single mode fibre probes are utilized to interface the grating couplers, injecting the optical signal from an O-band Santec tunable laser into the on-chip integrated amplifier on one side and collecting the amplified optical field on the other side. The collected optical power is split to two branches through a 10/90 splitter with the 10% channel feeding into an HP power meter and the other channel connecting to an optical spectrum analyser. The V-I response was firstly investigated, revealing a differential resistance of 3 Ω at a bias current of 130 mA, as shown in Fig.4. The on-chip gain is obtained by comparing the input and output waveguide-coupled power at the wavelength of interest after calibrating out the losses introduced by the grating couplers and the fiber-optics. Fig.5(a) shows the on-chip gain as a function of bias current for different waveguide-coupled input power. The device is transparent at 1292 nm, which is supposed to be around the gain peak at 40 mA. The on-chip gain increases with the bias current and reaches 6.5 dB at 110 mA, after that it shows a slight thermal roll-off behavior. The on-chip gain does not show obvious variation till the input power is above -5 dBm, as shown in Fig.5 (b).

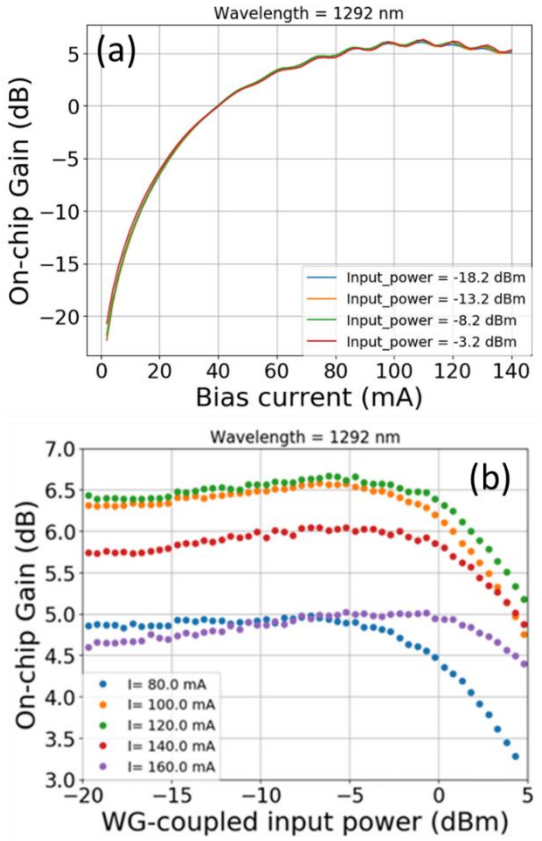

Fig.5 (a) Measured on-chip gain as a function of bias current for different waveguide-coupled input power at 1292 nm. (b) On-chip gain as a function of waveguide-coupled input power, showing slight variation when input power is below -5 dBm.

VI. Conculsion

We presented the full process flow for the µTP of GaAs QD devices on advanced SiPh platforms. Following this process flow, an array of O-band GaAs QD-on-Si optical amplifiers is demonstrated. The resulting devices show low resistance and exhibit up to 6.5 dB on-chip gain at 1292 nm. This work paves the way for the realization of GaAs QD lasers and/or complex on-chip optical systems by simply incorporating such integrated optical amplifiers in readily available Si PICs. Beside that µTP also shows great potential for the (co-) integration of a wide range of other optoelectronic components and even electronic circuits on SiPh substrates [6].

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Reference

[1] M. A. Meitl et al., "Transfer printing by kinetic control of adhesion to an elastomeric stamp," Nature Mater., vol. 5, pp. 33–38, 2006.

[2] D. Gomez, J. Thostenson, T. Moore, K. Oswalt, C. Reyes, R. Cok and A. Fecioru, "Micro Transfer Printing for Micro Assembly of Heterogeneous Integrated Compound Semiconductor Components, " in CS MANTECH Conference, May 9 -12, 2022.

[3] D. Gomez, K. Ghosal, M. A. Meitl, S. Bonafede, C. Prevatte, T. Moore, B. Raymond et al., "Process capability and elastomer stamp lifetime in micro transfer printing," In 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016.

[4] B. Corbett et al., “Transfer Printing for Silicon Photonics”, Semicond. Semimet. , vol. 99, pp.43-70, 2018.

[5] Europractice. Photonic integrated circuit prototyping and small volume production. https://www.imec-int.com/sites/default/files/imported/Photonic%2520integrated%2520circuit_EN_v4_MPW_yi_0.pdf

[6] G. Roelkens et al., "Micro-Transfer Printing for Heterogeneous Si Photonic Integrated Circuits," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 29, no. 3: Photon. Elec. Co-Inte. and Adv. Trans. Print., pp. 1-14, May-June 2023.