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Mathematical Design and Analysis of Three-Phase Inverters: Different Wide Bandgap Semiconductor Technologies and DC-Link Capacitor Selection

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Abstract: This paper introduces a mathematical design and analysis of three-phase inverters used in electric drive applications such as aerospace, electric vehicles, and pumping applications. Different wide bandgap (WBG) semiconductor technologies are considered in this analysis. Using SiC MOSFETs and Si IGBTs, two drive systems are developed in order to show the improvement in the efficiency of the inverter. The efficiency, total losses of the drive systems and the power losses of two inverters are computed and compared for both drive systems at the same operating condition. The drive system with SiC MOSFET shows much better performance compared to the drive system with Si IGBT. The SiC MOSFET system provides a 59.39%, 86.13%, and 29.76% lower conduction losses, switching losses and drive's total losses, respectively, compared to the Si IGBT system. The efficiency of the SiC MOSFET system is 2.46%pu higher than the efficiency of the Si IGBT drive system. Moreover, this paper introduces a detailed analysis for the dc-link voltage and current ripples in three-phase inverters. Furthermore, the minimal dc-link capacitor needed to deal with the ripple current and voltage is investigated. Finally, the performance of the drive with Si IGBT is experimentally tested under different operating speeds and loads.

Keywords: SynRM; modelling; simulation; conduction loss; inverter; SVPWM; switching loss; Si IGBT; SiC MOSFET; voltage ripples; current ripples; capacitor

MSC: 65K10

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1. Introduction

Due to their great efficiency and torque density, synchronous reluctance motor (SynRM) drive systems based on power electronics devices have recently received a lot of interest in contemporary applications. The performance of conventional silicon-based semiconductor devices has reached a bottleneck and has been challenging to further optimize in recent years despite their continued widespread use in industry [1]. Power converters are now being developed toward better efficiency, higher switching frequency, and higher power density due to the emergence of wide band gap (WBG) devices, which are represented by silicon carbide (SiC) and gallium nitride (GaN). WBG devices therefore have a very broad range of applications in some industries with significant demands for power converters, such as aerospace and electric vehicles (EV). However, the method for evaluating the switching performance of the devices in inverters needs to meet additional

standards as a result of the rising use of WBG devices. The classic voltage source inverter (VSI) has been more popular due to the unique needs of current source inverters for devices, hence there has been a lot of studies conducted on VSI's device switching characteristics [1] as well as modeling switching characteristics [2], calculating switching losses [3], and optimizing switching trajectories of devices [4]. Conventional motor drive inverters use industrial Si IGBTs and Si diodes with a standard maximum operating junction temperature of 125 °C for motor drive systems with a power rating of 60 kW [5]. The majority of the time, these inverters are attached to a heatsink that has an air- or water-cooling system. On account of the Si material, these systems' performance is almost at its limit. SiC devices are therefore receiving increased attention in motor drive systems. In reference [6], two 250 kW commercial VSI models for aerospace applications built on Si IGBTs and SiC MOSFETs are compared. In contrast to the Si IGBT-based design, the SiC MOSFETs VSI offers efficiency improvements while exhibiting acceptable electromagnetic interference (EMI) levels. The primary observed disadvantage is the apparent reduced dependability of SiC devices. Reference [7] compares two 190 kVA SiC- and Si-based industrial VSI projects for 690 V networks. The SiC-based proposal achieved higher efficiency with lower cost. Investigation and evaluation of the distinctive behavior of SiC-IGBT and Si-IGBT devices in VSI under resistive and R-L loads is performed in reference [8]. Higher switching speed, lower switching loss, and higher efficiency are achieved with SiC-IGBT switches. A performance of three different 6 kW inverter topologies based on SiC MOSFETs is compared in reference [9]. It highlights the importance of considering modulation technique, deadtime value and their effects on various converter components, such as total losses. Several energy conversion solutions in medium voltage using 3.3 kV- [10], and 10 kV- [11] SiC MOSFET switches are discussed in references [10] and [11], respectively. The dynamic features of 1.2 kV SiC MOSFET switch are investigated in reference [12]. At very high temperatures, switch maintains exceptional dynamic properties. However, these findings do not provide a comparison between the SiC and Si power devices. In reference [13] a dynamic behavior of SiC IGBT is studied and compared with Si IGBT at the same rated voltage. SiC-IGBT has a lower equivalent on-resistance than Si-IGBT and is better suited for applications needing high voltage and current operation. VSIs based on SiC MOSFETs and Si devices fed motor drive systems are introduced in references [14–16]. According to these studies, SiC power devices prove higher efficiency than Si devices.

The dc-link capacitor represents another important issue affecting the performance of the motor drive system. The dc-link capacitor absorbs the harmonic currents that tend to indicate the presence of the dc bus voltage ripple. To reduce the dc-link voltage ripple, the capacitor is essential to the proper operation of a three-phase VSI [17]. To further decrease EMI caused by the switching processes, a dc-link current ripple must be limited. The dc-link voltage ripple can be reduced by using a greater capacitance value. However, this increases the capacitor volume and cost, which lowers the inverter's power density and tends to cost more per kilowatt. Therefore, selecting the optimal value of the dc-link capacitor is crucial to the VSI's functionality. The proper design of the dc-link capacitor depends on the accurate estimates of its voltage and current ripples. The values of these ripples are dependent on the pulse width modulation (PWM) switching method [18–25]. Obtaining the peak *rms* current ripple in the dc-link capacitor using computation method is introduced in references [18,19]. According to these researches, the *rms* ripple current is a function of modulation index and phase displacement. In references [20,21], the impact of dead time on the value of the input current ripple of three-phase VSI is considered. Determination of the *rms* input current using direct current control scheme is invented in reference [22]. The maximum voltage ripple must be considered when sizing the dc-link capacitor, especially when the equivalent series resistance of the capacitor is low, and the smaller value of the capacitor is consequently enough to manage ripple current stress. The dc-link capacitor voltage ripple reduction methods for multilevel converter are discussed in references [23,24]. In reference [25], calculation of VSIs' dc-link voltage ripple

considering reverse recovery of antiparallel diodes is displayed. The impact of load imbalance in VSI on capacitor voltage ripple is confirmed in references [26–28]. Calculation of the theoretical value of the dc-link capacitor voltage ripple using voltage control scheme is proposed in reference [29]. Investigation of the capacitor voltage ripple of VSI under non-linear output current is shown proposed in reference [30]. However, these papers do not mention the change in the power factor and modulation index on the peak *rms* voltage ripple value. The variation in the power factor and modulation index on the voltage ripple is discussed in reference [31].

In this paper, a mathematical design and analysis of three-phase inverters used in electric drive applications such as aerospace, electric vehicles and pumping applications is investigated. Different WBG semiconductor technologies are considered in the design of the inverter. Then, two synchronous reluctance motor drive systems with standard two-level inverters are created using traditional Si IGBT and SiC MOSFET, respectively, in order to evaluate the benefits of SiC devices in drive applications. Furthermore, the power losses of inverters with space vector pulse width modulation (SVPWM) control are estimated and studied for both drive systems. This paper also includes a full analysis of the dc-link voltage and current ripples. In addition, the minimum dc-link capacitor required to cope with the ripple current and voltage is evaluated. Finally, the three-phase SynRM drive's performance is experimentally evaluated under various operating speeds and loads.

2. Drive System Comparison with Si IGBT and SiC MOSFET

This section compares different WBG semiconductors technologies for three-phase inverters. This is achieved by comparing the performance of three-phase synchronous reluctance motor drive systems using different WBG semiconductor technologies. Using SiC MOSFETs and Si IGBTs, two 5.5 kW synchronous reluctance motor driving systems are developed in order to offer a reasonable measure of the system improvement. The efficiency, total losses of the drive systems and the power losses of two inverters are computed and compared for both drive systems at the same operating condition. The specification of the two drive systems, e.g., motor specification, inverter switches and SVPWM and the performance comparison of the two drives are introduced in this section.

2.1. Electric Motor

The electric motor in both drives is a three-phase SynRM of 5.5 kW, 4 poles and 36 slots. The rated condition of this motor is 3000 rpm and 17.3 A (max. value). The average torque, motor losses and efficiency of this motor at rated condition and at optimal current angle (55°) are 17.23 N.m, 290.9 W and 94.88%, respectively [32]. The performance of this motor is investigated with different inverter semiconductor technologies, e.g., Si and SiC.

2.2. Three-Phase Two-Level Inverter

A three-phase two-level VSI is used. In the first drive system, the inverter has six Si IGBTs [33] as shown in Figure 1a, whereas the inverter in the second drive system consists of six SiC MOSFETs [34] as shown in Figure 1b. The difference between the two semiconductor technologies is summarized in Figure 2, and their data sheets can be found in [33,34]. Figure 2a,b show the forward characteristics of the SiC MOSFET and Si IGBT and their body diode. It is demonstrated from Figure 2a,b that the SiC MOSFET has lower forward voltage at the same current level compared to that of Si IGBT. As a result, the SiC MOSFET provides a lower conduction loss compared to Si IGBT as will be discussed in the next section.

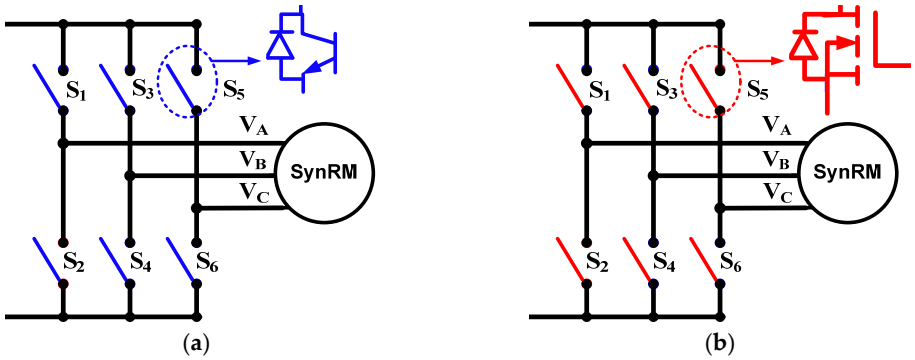


Figure 1. (**a**) Si IGBT drive system and (**b**) SiC MOSFET drive system.

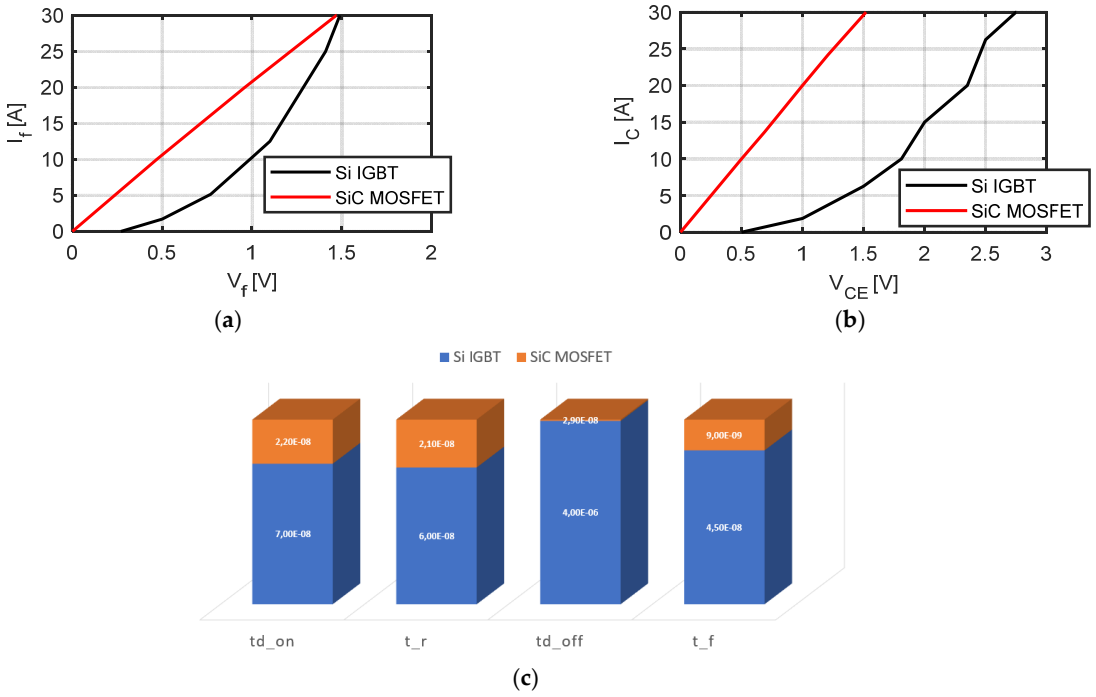


Figure 2. Comparison between Si IGBT and SiC MOSFET (**a**) forward characteristics of body diode, (**b**) forward characteristic for switch, and (**c**) on and off delay, rise and fall time [33,34].

As shown in Figure 2a, SiC MOSFET has much lower on and off time compared to Si IGBT. The delay on time and rise time of the SiC MOSFET are 68.6% and 65% lower, respectively, compared to those of Si IGBT. In addition, the delay off time and fall time of the SiC MOSFET are much lower compared to those of Si IGBT. The delay off time of SiC MOSFET is 3448% lower compared to that of Si IGBT and the fall time of the SiC MOSFET is 111% lower compared to that of Si IGBT. In addition, Figure 3 shows that the turn on and off energy losses are much lower in the case of the SiC MOSFET compared to that of the Si IGBT. The significant reduction in the turn on and off energy loss of the SiC MOSFET enables them to provide much lower switching losses, as is presented in the next section.

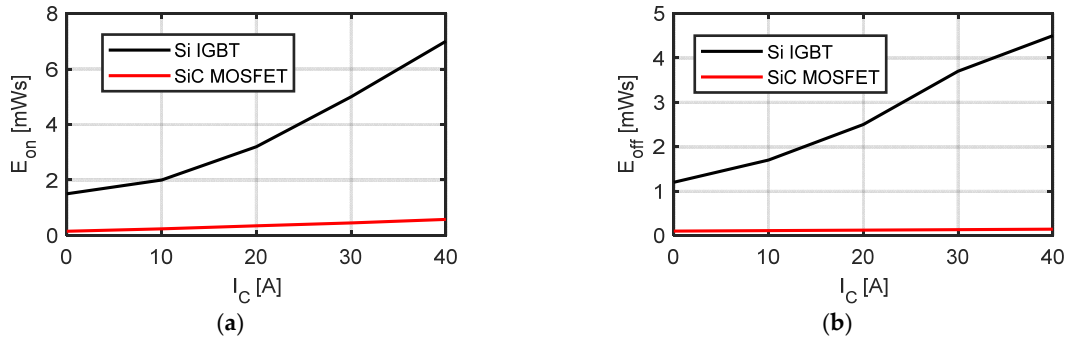
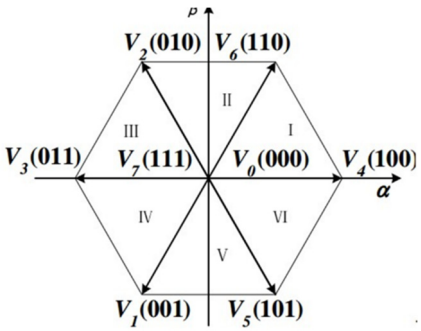


Figure 3. Comparison between Si IGBT and SiC MOSFET (**a**) turn on, (**b**) turn off energy loss [33,34].

2.3. SVPWM and Inverter Losses

In this part, the SVPWM and the calculation of switching and conduction losses of the inverter are discussed. According to Figure 1, the three-phase inverter consists of six switches. These switches are only configured in eight different ways to prevent output short-circuiting through any of the three half-bridge terminals, and the load from open-circuiting at any instant. There are six active voltage vectors (V_1–V_6) and two zero output voltage vectors (V_0 [000], V_7 [111]) among the eight allowed combinations as demonstrated in Figure 4a. Consistent with the voltage vector V_0 (000), the top switches in the inverter are off and the bottom switches are on. The reference output voltage of the inverter is computed using the neighbouring active vectors and zero vector in each sector. The duty cycles of these vectors are calculated as in (1). In (1), the entire duration periods of vectors $V_{\alpha,}$ V_β and zero vector are $T_{\alpha,}$ T_β and T_z, respectively; θ_v and m_v denote the angle of the reference output vector inside the hexagonal sector and the modulation index, respectively. The switching sequence of the SVPWM is displayed in Figure 4b [35].

$$V_o^* = d_\alpha V_\alpha + d_\beta V_\beta + d_z V_z, \quad \begin{cases} d_\alpha = \dfrac{T_\alpha}{T_s} = m_i * \sin\left(\dfrac{\pi}{6} + \theta_v\right) \\ d_\beta = \dfrac{T_\beta}{T_s} = m_i * \sin(\theta_v) \\ d_7 = d_0 = \dfrac{T_z}{T_s} = 1 - (d_\alpha + d_\beta) \end{cases} \quad (1)$$



(**a**) (**b**)

Figure 4. (**a**) Hexagon for three-phase inverter and (**b**) switching sequence for continuous SVPWM for one cycle in the first sector.

The efficiency is easily determined using the computed output power and the total estimated losses, which include the machine's copper and iron losses as well as the switching and conduction losses of the inverter. In this comparison, the mechanical losses are disregarded. On the other hand, using the machine's observed winding resistance and current amplitude, it is simple to calculate the SynRM copper losses. Resistance is measured at temperature of 70 °C (resistivity = 0.0217ohm mm²/m).

The efficiency of the drive system is given by

$$\eta = \frac{P_o}{P_o + P_{cu} + P_{iron} + P_{inverter}}, \quad (2)$$

where P_o is the motor's mechanical output power, which is determined using the FEM model's estimated torque by

$$P_o = T_e * \omega_r. \quad (3)$$

Based on Bertotti's statistical loss theory, iron losses in the SynRM are computed. The following are the ways in which the theory is dependent on loss separation into excess, hysteresis, and classical eddy current losses:

$$P_{iron} = P_h + P_c + P_e. \quad (4)$$

Figure 5 shows the calculation of the conduction losses and switching losses in the top switch in first leg. In Figure 5, the red signal represents the current flowing in the switch and the blue signal represents the voltage between switch terminals. The switching losses are represented by the green signal, and the black signal at the bottom represents the conduction losses in the switch. The switching losses and the conduction loss are calculated as the mean value of the green signal and the black signal in Figure 5 over one complete period of the fundamental frequency. This is given by (5). In (5), V_S and V_D represent the voltage between the switch terminal and the diode terminals, respectively, whereas I_S and I_D represent the current flowing through the switch diode, respectively. In (5), P_{s_loss} represents the conduction losses and the switching of one switch, and the total loss ($P_{inverter}$) is obtained by adding the switching losses and the conduction losses of all switches. This is achieved by selecting the corresponding voltage and current for each component for each loss type.

$$P_{s\_loss} = \frac{1}{T}\left\{\int_0^T V_S * I_S \, dt + \int_0^T V_D * I_D \, dt\right\}. \quad (5)$$

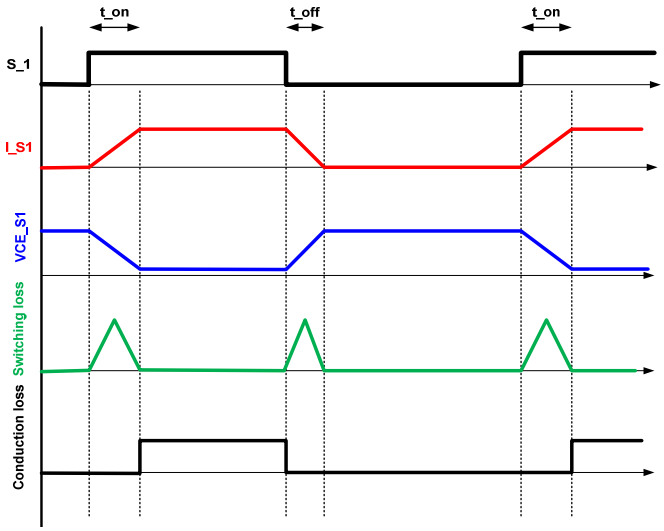


Figure 5. Calculation of switching and conduction losses.

2.4. Drive System Performance Comparsion with Si IGBT and SiC MOSFET

In this section, two SynRM drive systems of 5.5 kW, four poles, 3000 rpm and 17.3 A (max) are used to investigate the features of the SiC MOSFET in comparison to Si IGBT. The performance of the three-phase SynRM has been studied in [36] without considering the type of inverter switches or losses. The performance of the two drive systems is compared at rated condition and at optimal current angle (55°). Note that the two drive systems have the same optimal current and the same rated condition. The only difference between the two systems is the type of inverter's switch. Figure 6a,b compare the conduction losses and the switching losses at rated condition and at optimal current angle,

respectively. It is demonstrated from Figure 6 and Table 1 that the SiC MOSFET system has 59.39%, 86.13%, and 29.76% reduced conduction losses, switching losses, and total drive losses when compared to the Si IGBT system. The efficiency of the SiC MOSFET system is 2.46% pu greater than that of the Si IGBT driving system. Figure 7 compares the conduction losses, switching losses, total losses, and efficiency of the two systems at different line currents, optimal current angles, and rated speed. Figure 8 shows the current waveforms of the motor and switches and diodes of the inverter at rated condition.

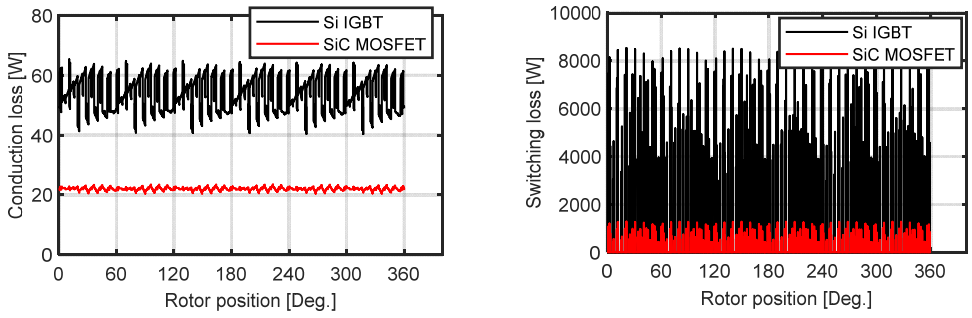


Figure 6. (**a**) Conduction losses and (**b**) switching losses versus rotor position at rated condition and at optimal current angle.

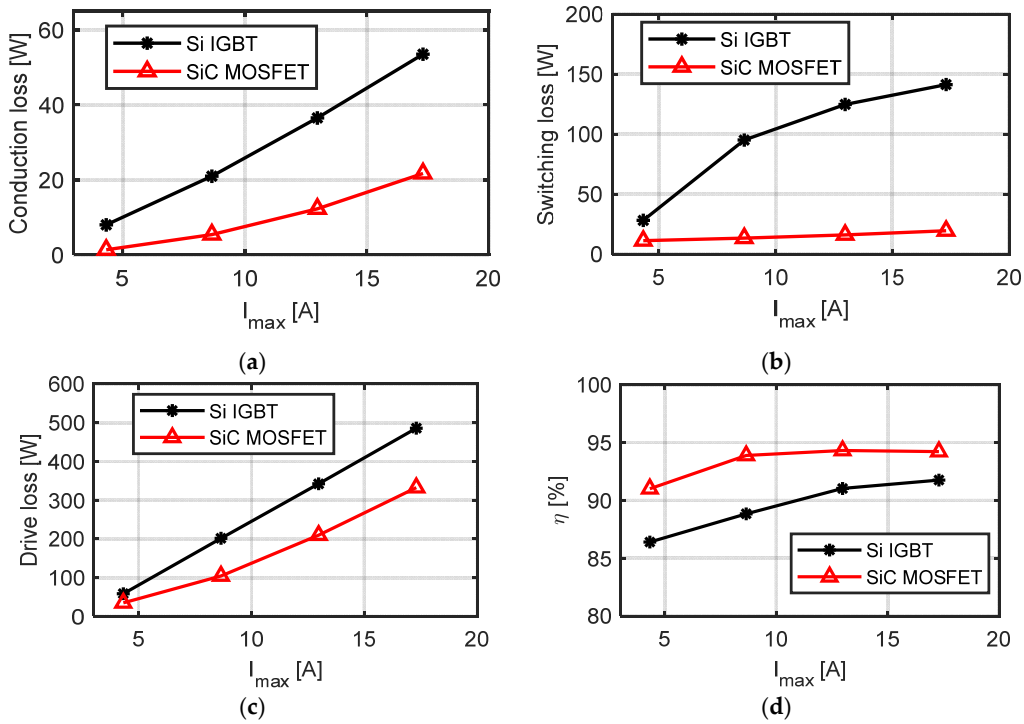


Figure 7. (**a**) Conduction losses, (**b**) switching losses, (**c**) total drive losses and (**d**) efficiency at different line currents, optimal current angles, and rated speed.

Table 1. Comparison of losses and efficiency between Si IGBT and SiC MOSFET at rated condition.

	Si IGBT	SiC MOSFET
Switching losses (W)	141.41	19.61
Conduction losses (W)	53.53	21.74
Motor losses (W)	290.90	290.90
Total losses for drive (W)	485.84	341.27
Drive system efficiency (%)	91.76	94.22

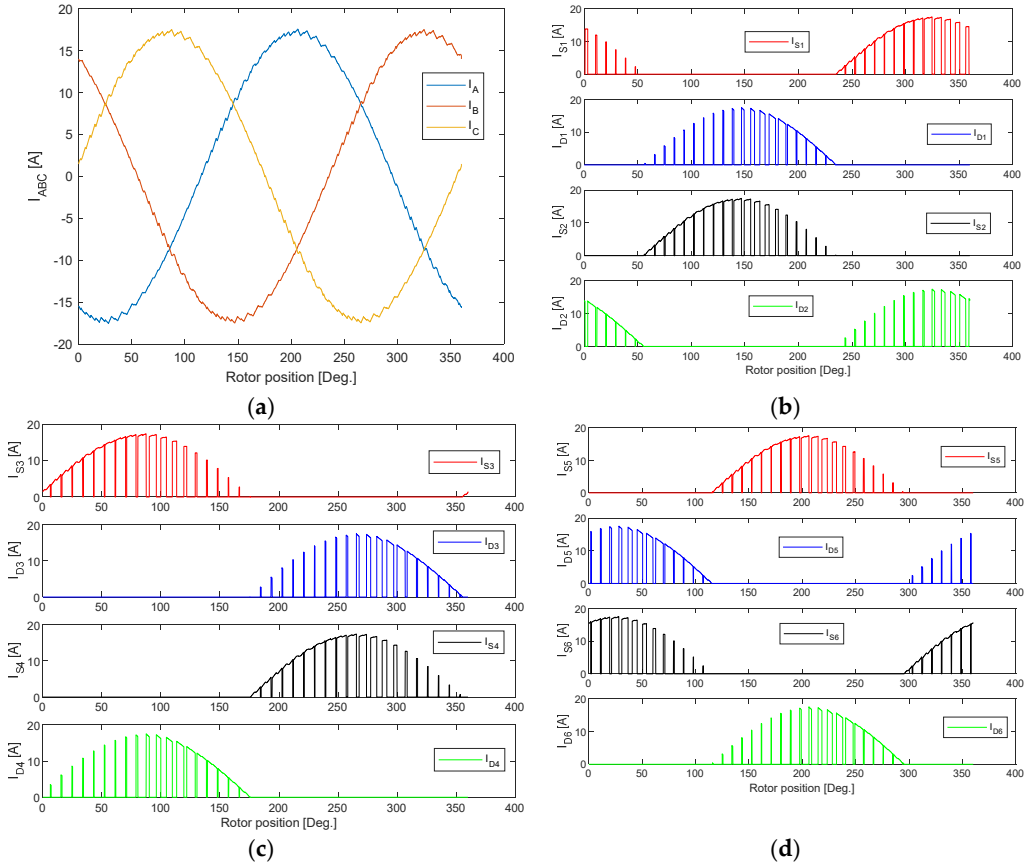


Figure 8. (**a**) Three−phase currents, (**b**) currents in the first leg, (**c**) second leg and (**d**) third leg of inverter at rated condition and optimal current angle.

3. Design of the dc-Link Capacitor

This section discusses the optimal dc-link capacitor design to overcome voltage and current sags in the dc-link. The discussion starts with an analysis of the dc-link voltage ripple. The analytical computation of the current ripples in a dc connection is then examined. The ideal capacitance of the dc-link callus is then computed.

3.1. Analysis of Voltage Ripple

This section analyzes the voltage ripple in the dc-link of the two-level inverter. Figure 9 shows the configuration of the two-level three-phase inverter with the dc-link capacitor and the three-phase SynRM. The three-phase motor current can be described as follows:

$$i_A = I_m \cos(\omega t - \emptyset), \tag{6}$$

$$i_B = I_m \cos\left(\omega t - \emptyset - \frac{2\pi}{3}\right), \tag{7}$$

$$i_C = I_m \cos\left(\omega t - \emptyset + \frac{2\pi}{3}\right), \tag{8}$$

where I_m, ω, t and $\emptyset$ represent the peak current of the motor in A, angular frequency in *rad*/*s*, time in *s* and the power factor of the motor, respectively.

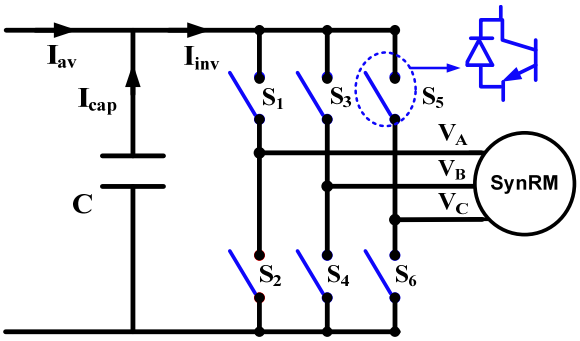


Figure 9. Two-level inverter with dc-link capacitor.

The analysis in this section is introduced considering SVPWM that has been presented in Section 2.3. The duty cycles of the top switches of the inverter can be represented as follows:

$$D_A = \frac{1}{2} + \frac{1}{2} m_i \cos\left(\omega t - \frac{\pi}{6}\right), \quad (9)$$

$$D_B = \frac{1}{2} - \frac{\sqrt{3}}{2} m_i \cos\left(\omega t + \frac{\pi}{3}\right), \quad (10)$$

$$D_C = \frac{1}{2} - \frac{1}{2} m_i \cos\left(\omega t - \frac{\pi}{6}\right), \quad (11)$$

where m_i represents the modulation index of the inverter controlled by the SPWVM. It has a maximum value of 1 and it can be calculated by (12). In (12), V_{Line} and V_{DC} represent the peak value of the line-to-line voltage and the dc-link voltage, respectively.

$$m_i = \frac{V_{Line}}{V_{DC}}. \quad (12)$$

The inverter current (I_{inv}) can be calculated using the switching states of the inverter top switches and the motor currents as follows:

$$I_{inv} = S_1 i_A + S_3 i_B + S_5 i_C. \quad (13)$$

Considering a lossless operation of the inverter, the power in the dc-link or exiting from the battery is equivalent to the input power to the three-phase SynRM as given by (14). Then, the average current (I_{av}) of the inverter which is exiting from the battery can be given by (15).

$$V_{DC} I_{av} = \frac{\sqrt{3}}{2} V_{line} I_m \cos \emptyset, \quad (14)$$

$$I_{av} = \frac{\sqrt{3}}{2} m_i \, I_m \cos \emptyset. \quad (15)$$

Considering the circuit shown in Figure 9, the capacitor current (i_{cap}) can be calculated as follows:

$$I_{cap} = I_{inv} - I_{av.} \quad (16)$$

The fundamental formula for the current flowing through a capacitor (i_{cap}) is defined as follows:

$$i_{cap} = C \frac{dv_{cap}}{dt}. \quad (17)$$

Then, the voltage ripple across the capacitor can be derived as follows:

$$dv_{cap} = \Delta V = \frac{i_{cap}\, dt}{C}. \quad (18)$$

Formula (18) demonstrates that the voltage ripple (ΔV) for a particular capacitor is proportional to the Amp-sec ($i_{cap}\, dt = C\Delta V$). By determining an appropriate Amp-sec formula, one may derive an exact expression for the minimal dc-link capacitance necessary for a specified voltage ripple criterion.

Figure 10 displays the switching diagram and corresponding current and voltage waveforms for the top transistors on each leg of the inverter. It is clearly seen from Figure

10 that there is no current flowing through the inverter in the zero switching states (0 0 0) and (1 1 1). According to the symmetric in voltage ripples in Figure 10, the following equations for Amp-sec for various switch combinations are demonstrated:

$$C\,\Delta V_1 = -\frac{1}{2}T_s(1 - D_A)I_{av}, \tag{19}$$

$$C\,\Delta V_2 = \frac{1}{2}T_s(D_A - D_B)(I_A - I_{av}), \tag{20}$$

$$C\,\Delta V_3 = \frac{1}{2}T_s(D_B - D_C)(I_A + I_B - I_{av}), \tag{21}$$

$$C\,\Delta V_4 = -\frac{1}{2}T_s\,D_C\,I_{av}, \tag{22}$$

where T_s represents the switching time $(\frac{1}{F_{sw}})$ and F_{sw} is the switching frequency.

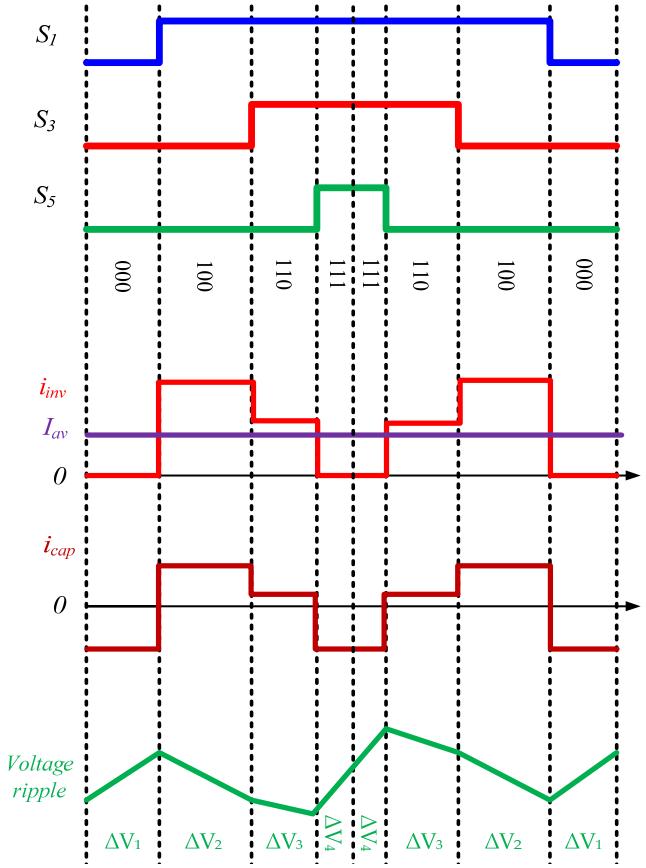


Figure 10. Top switch switching states, inverter, capacitor current and voltage ripple.

Then, the goal is to calculate the maximum Amp-sec in a given sector using the power factor and the modulation index. The maximum ampere sec (voltage ripple max $[\Delta V_{max}]$) can be determined from one of the following expressions $C\,(\Delta V_3 + \Delta V_4)$ or $C\,\Delta V_4$ and these expressions can be described as follows:

$$C\,\Delta V_4 = -\frac{\sqrt{3}}{8}\,m_i\;\;I_m\,T_s\left[1 - m_i\;cos\left(\omega t - \frac{\pi}{6}\right)\right]cos\,\emptyset, \tag{23}$$

$$C\,(\Delta V_3 + \Delta V_4) = m_i\;\;I_m\,T_s\left[\frac{1}{2}\sin\omega t * \cos\left(\omega t - \frac{\pi}{3} - \emptyset\right) - \frac{\sqrt{3}}{8}\cos\emptyset * \left(1 - m_i\;\cos\left(\omega t - \frac{\pi}{6}\right) + 2m_i\;\sin\omega t\right)\right]. \tag{24}$$

For sector 1, the maximum value of $|\mathrm{C}\,\Delta V_4|$ is obtained at unity power factor $(cos\,\emptyset = 1)$, $\omega t = 0$ or $\frac{\pi}{3}$ and modulation index of $\frac{1}{\sqrt{3}}$. The maximum value of $|C\,\Delta V_4|$ is given by (25). To obtain the maximum value of $|C\,(\Delta V_3 + \Delta V_4)\,|$, a 3D plot is used as there is no closed form solution in terms of power factor and the modulation index. A 17.3 A peak current is used to obtain the 3D plot shown in Figure 11.

$$|C\ \Delta V_4|_{max} = \frac{I_m\ T_s}{16} \tag{25}$$

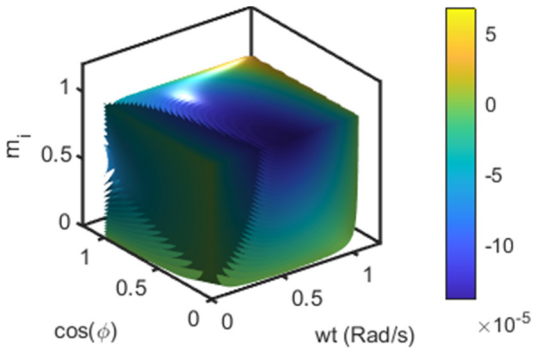


Figure 11. 3D MATLAB plot of $|C\ (\Delta V_3 + \Delta V_4)\,|$ at 15 kHz switching frequency and 17.3 A peak motor current versus power factor, modulation index and ωt.

3.2. Analysis of Current Ripple

This section analyses the current ripple in the dc-link capacitor. Figure 10 is used in the ripple current analysis. The switching periods d_α and d_β for switching between the states of (1 0 0) and (1 1 0) are given by (1) and described in Figure 12. The formulas described in (26 and 27) are expressions to calculate the for the inverter input current's average value. The final value of the average current described in (27) gives the same result described in (15). In the same way, the *rms* value of the inverter current can be obtained as shown in (28) and (29).

$$I_{av} = d_\alpha\ \ i_A + \ \ d_\beta(\,i_A + i_B) = d_\alpha i_A - \ \ d_\beta\, i_C, \tag{26}$$

$$\begin{aligned} I_{av} &= m_i\, cos\left(\omega t + \frac{\pi}{6}\right) * I_m\, cos(\omega t - \emptyset) - m_i\, sin(\omega t) * I_m\, cos\left(\omega t - \emptyset + \frac{2\pi}{3}\right) \\ &= \frac{1}{2} m_i * I_m \left\{ cos(\emptyset) * \frac{\sqrt{3}}{2} - sin(\emptyset) * \frac{1}{2} - sin(\emptyset) * -\frac{1}{2} + cos(\emptyset) * \frac{\sqrt{3}}{2} \right\} \\ &= \frac{1}{2} m_i * I_m \left\{ 2 * cos(\emptyset) * \frac{\sqrt{3}}{2} \right\} = \frac{\sqrt{3}}{2} m_i * I_m * cos(\emptyset), \end{aligned} \tag{27}$$

$$i^2_{rms} = \ d_\alpha\ \ i^2_A + \ \ d_\beta\ \ i^2_C \tag{28}$$

$$\begin{aligned} i^2_{rms} &= m_i \cos\left(\omega t + \frac{\pi}{6}\right) * I^2_m\, cos^2(\omega t - \emptyset) + m_i \sin(\omega t) * \ I^2_m\, cos^2\left(\omega t - \emptyset + \frac{2\pi}{3}\right) \\ &= \frac{m_i * I^2_m}{2} * \left\{ cos\left(\omega t - \frac{\pi}{6}\right) - \frac{1}{2} sin(3\omega t - 2\emptyset) + cos\left(\omega t - \frac{\pi}{6} - 2\emptyset\right) \right\} \\ &= \frac{m_i * I^2_m}{2\pi} * \left\{ \frac{3}{2} + \frac{3}{2} - \frac{1}{2}\cos(2\emptyset) - \frac{1}{2}\cos(2\emptyset) + 3 * \sin\left(\frac{\pi}{6} - 2\emptyset\right) + 3 * \sin\left(\frac{\pi}{6} + 2\emptyset\right) \right\} \\ &= \frac{m_i * \mathrm{I}^2_{\mathrm{m}}}{2\pi} * \{1 + 4 * \cos^2(\emptyset)\}. \end{aligned} \tag{29}$$

Then, the capacitor current can be calculated as follows:

$$I^2_{c,rms} = \ I^2_{rms} - I^2_{av} = \frac{m_i * I^2_m}{2\pi} * \{1 + 4 * cos^2(\emptyset)\} - \frac{3}{4} {m_i}^2 * I^2_m * cos^2(\emptyset), \tag{30}$$

$$I_{c,rms} = I_m \sqrt{\frac{m_i}{2\pi} * \left[1 + cos^2(\emptyset) * \left(4 - \frac{3\pi}{2} m_i\right)\right]}. \tag{31}$$

The RMS ripple dc-link current is given as follows:

$$\text{RMS Ripple dc-link current } = \frac{I_{c,rms}}{I_{m,rms}} = \sqrt{\frac{M}{\pi} * \left[1 + cos^2(\emptyset) * \left(4 - \frac{3\pi}{2} M\right)\right]}. \tag{32}$$

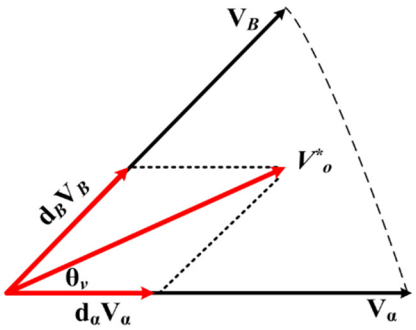
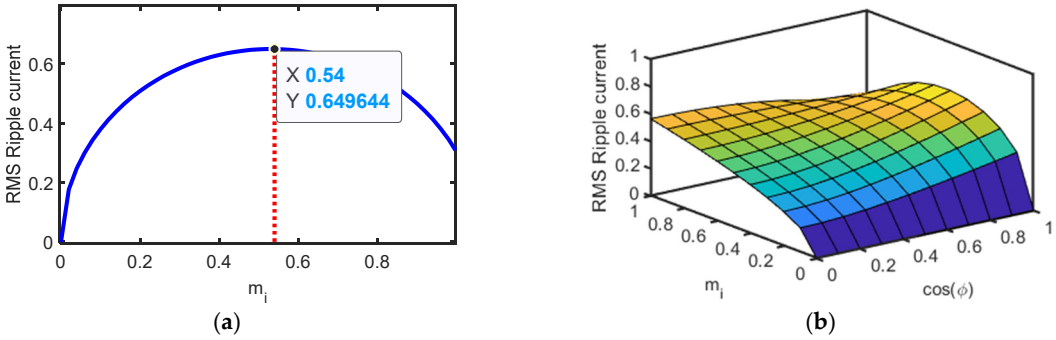


Figure 12. Reference voltage located in the first sector.

Figure 13a shows the RMS ripple current at unity power factor and at different modulation index. It has been determined from Figure 13a that the maximum ripple current occurs at a modulation index of 0.54. However, the operation of the three-phase SynRM at unity power factor is not a real operation point. Hence, the RMS ripple current has been plotted as a function of both power factor and modulation index as shown in Figure 13b. The maximum value of RMS ripple current occurs at modulation index of 0.5 and unity power factor. This is also not a real operating point. Hence, the operating point that will be considered in the calculation is the point that provides the maximum output power. For the considered SynRM, a 17.3 A peak current, modulation index of 0.7244 and power factor of 0.6176 provide the maximum power. Then, the RMS ripple current is 6.5 A.



(**a**) (**b**)

Figure 13. RMS ripple current at (**a**) versus modulation index and at unity power factor and (**b**) versus modulation index and power factor.

4. Results and Discussion

4.1. Optimal dc-Link Capacitance

In this section, the type of the DC link capacitor and its voltage rating are investigated. First, the minimum capacitance required for the maximum voltage ripple is investigated. Then, the calculated values of capacitance are checked for the RMS ripple current. The minimum capacitance that can sustain the maximum voltage ripple is as in (33). The value of $|C\ \Delta V|_{Max}$is the maximum value of this vector $[|C\ \Delta V_4|_{max}, max\ of\ 3D\ plot]$. In (33), $V_{ripple,max}$ is the allowed peak ripple voltage which can be set to ±2.5% of V_{DC}. For 600 V dc-link voltage, the value of $V_{ripple,max}$ is 30 V. For the three-phase SynRM introduced in [32], the peak current of the motor is 17.3 A. Then, the value of $|C\ \Delta V_4|_{max}$ is 7.2083 × 10^{-5} and the maximum value of the 3D plot is 7.2076 x10^{-5}. Hence, $|C\ \Delta V|_{Max}$ is 7.2083 × 10^{-5}. Then, the minimum-capacitance required to keep voltage ripple under ±2.5% of the dc-link voltage is $4.8\ \mu F$ as given by (34). However, this is not the final value as it is guaranteed that this capacitance can handle the current ripple in the dc-link.

$$C_{min} = \frac{2 * |C\ \Delta V|_{Max}}{V_{ripple,max}}, \quad (33)$$

$$C_{min} = \frac{2 * 7.2083 * 10^{-5}}{30} = 4.8\ \mu F. \quad (34)$$

The voltage rating of the capacitor should always be at least twice (or 1.5 times) the highest voltage that might possibly be present in the circuit. For a 600 dc-link voltage, a dc-link capacitor with 900 V rating and $4.8\ \mu F$ is initially selected. There are three types of dc-link capacitors that are often used in electric drives, including multi-layer ceramic capacitors, metallized polypropylene film capacitors, and aluminium electrolytic capacitors. Table 2 compares the relative performance of the three dc-link capacitors [37]. The film capacitor is preferable in the high dc-link ripple currents. A $5\ \mu F$, 920 V film capacitor is chosen [38]. This capacitor can withstand a 9 A maximum ripple current which is greater than the maximum RMS ripple current calculated in the previous section (6.5 A). Moreover, this capacitor offers a 28.83 V ripple voltage which is lower than ±2.5% of V_{DC}.

Table 2. Comparison between the relative performance of different dc-link capacitors [37].

	Ceramic Capacitors	**Film Capacitors**	**Electrolytic Capacitors**
Capacitance	inferior	medium	preferable
Voltage rating	inferior	preferable	medium
Ripple current	medium	preferable	inferior
Frequency	preferable	preferable	inferior
Reliability	preferable	preferable	inferior
Temperature	preferable	inferior	medium
Cost	inferior	Medium	preferable

4.2. Experimental Results

The experimental setup depicted in Figure 14 is utilized to evaluate the experimental performances of the three-phase drive system which consist of a Si IGBT and 36 slots, four poles, and 5.5 kW SynRM. A three-phase 10 kW induction motor is linked to the three-phase SynRM. To measure the SynRM torque, a Lorenz torque sensor is installed in the connection between the two machines. An incremental encoder installed in the induction motor's rotor is used to measure speed. The induction motor is used to regulate the speed of the three-phase SynRM while it is in torque control mode of operation. The three-phase SynRM is managed by a three-phase inverter with 6.6 kHz switching frequency. In addition, 600 V is the DC bus voltage. The inverter regulating pulses are produced using digital signal processing (DSP1103) using a space vector pulse width modulation with field-oriented control. Figure 15a,b compare the measured drive losses and efficiency, respectively, with the simulated results of the drive system at rated speed, optimal current angles, and different currents and at two different switching frequencies, e.g., 6.6 kHz and 15 kHz. Note that the mechanical losses have not been considered in the simulation results. As a result, there is some mismatch between the simulation results and the experimental results at the same switching frequency (6.6 kHz). The mismatch between the simulated and measured total losses and efficiency at rated condition, optimal current angle and 6.6 kHz switching frequency is about 16% and 1.33%, respectively. A good agreement between the simulated at 15 kHz and measured results at 6.6 kHz is detected in this comparison, which validates the theoretical comparison introduced in this paper. The agreement has been achieved because the measured results at 6.6 kHz include the mechanical losses, which is not included in the simulation results at 15 kHz. In addition, the simulation results at 15 kHz have about 55% higher switching losses than the simulation results at 6.6 kHz as shown in Table 3. Table 3 compares the simulation results of the Si IGBT and SiC MOSFET at different switching frequencies, rated conditions and optimal current angles.

Table 3. Comparison between the simulated performance of Si IGBT and SiC MOSFET at rated condition and at different switching frequency.

	Si IGBT		SiC MOSFET	
Switching Frequency	**At 15 kHz**	**At 6.6 kHz**	**At 15 kHz**	**At 6.6 kHz**
Switching losses (W)	141.41	63.68	19.61	11.86
Conduction losses (W)	53.53	53.57	21.74	21.74
Motor losses (W)	290.90	290.90	290.90	290.90
Total losses for drive (W)	485.84	408.15	341.27	324.5
Drive system efficiency (%)	91.76	92.98	94.22	94.34

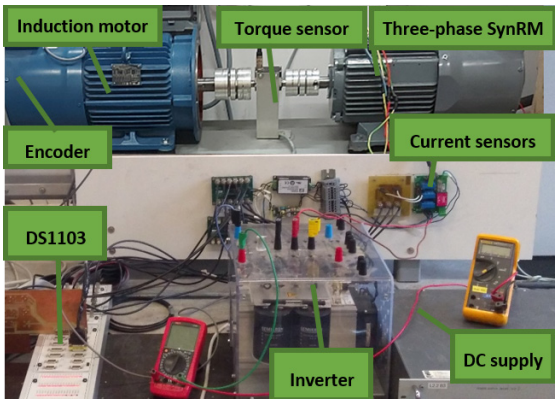


Figure 14. Photo of experimental setup of the drive system.

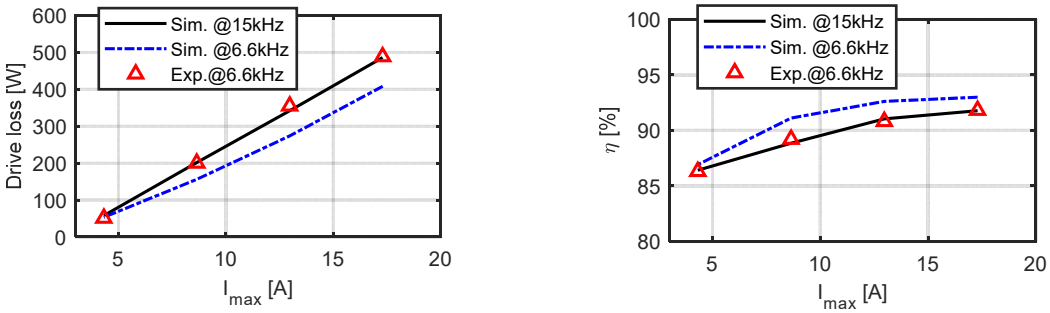


Figure 15. (**a**) Measured total losses and (**b**) measured efficiency at different loads, at rated speed and at optimal current angles for the drive system with Si IGBT.

For various rotor speeds, various line currents, and optimal current angles, the measured losses and efficiency maps of the whole drive system are shown in Figure 16a and b, respectively.

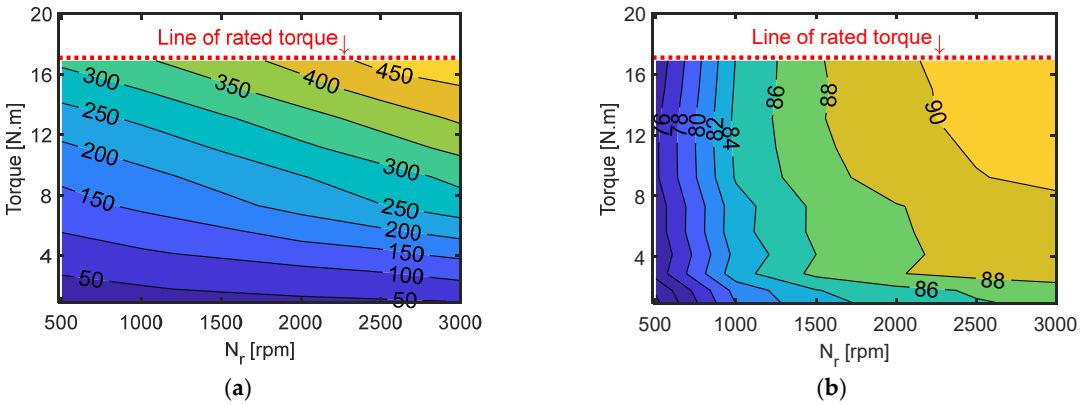


Figure 16. Drive system with Si IGBT (**a**) measured losses map and (**b**) measured efficiency map at different loads, at different speed and at optimal current angles.

5. Conclusions

This paper introduced the mathematical design of three-phase inverters. Different types of WBG switches were considered. This paper compared two SynRM drive systems with SiC MOSFET and Si IGBT. The SiC MOSFET showed much better performance compared to the Si IGBT. The efficiency of the SiC MOSFET system is 2.46%pu higher than that of the Si IGBT drive system. The power losses of inverters controlled by space vector pulse width modulation (SVPWM) were computed and analyzed in this work for both drive systems. The comparison was carried out at different loads and at different switching frequencies, e.g., 6.6 kHz and 15 kHz. When compared to the Si IGBT system and at 15 kHz switching frequency, the SiC MOSFET system had 59.39%, 86.13%, and 29.76% reduced conduction losses, switching losses, and drive total losses. With the decrease in the switching frequency, the switching losses were reduced for both technologies; however, they significantly reduced in case of the Si IGBT. For the Si IGBT and the SiC MOSFET, the switching losses at switching frequency of 6.6 kHz was 55% and 39.5% lower, respectively, than their values at 15 kHz. The considered motor (SynRM) had no winding, cages or magnet in the rotor. Therefore, the temperature rise was lower compared to that of other types of electric machines such as induction machine. For the inverter with SiC MOSFTE, the losses were lower than for the Si IGBT. Therefore, the temperature rise was lower in SiC MOSFTE compared to that of Si IGBT. Moreover, the performance of the three-phase SynRM drive was tested at varied operating speeds and loads. This article also included a thorough assessment of the dc-link voltage and current ripples. Moreover, the minimum dc-link capacitor required to accommodate the ripple current and voltage was calculated.

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