DAC Young Fellows

Update Logic Synthesis objectives for better Placement and Routing

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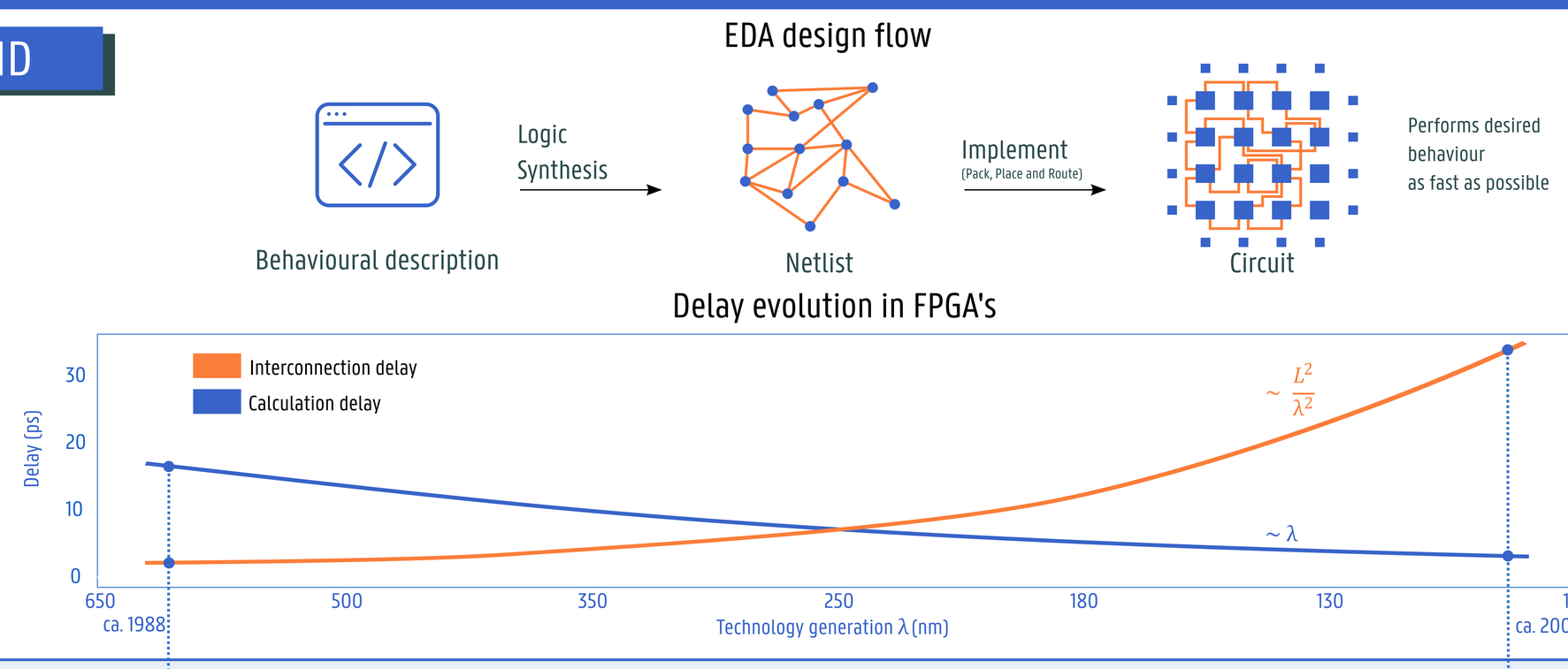
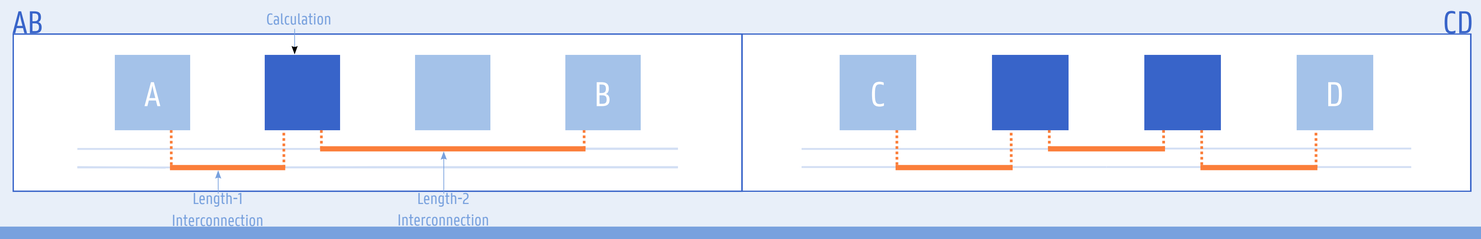
BACKGROUND



PROBLEM

1. Compare the following two routes AB and CD



2. Which route is fastest?

Answer changed over time

In the past: AB is faster!

Calculation delay >> Interconnection delay

A calculation block has unit delay of 1 = 1

So, these are the delays for AB and CD

AB: 1x → AB = 1

CD: 2x → CD = 2

Now: CD is faster!

Interconnection delay >> Calculation delay

These are the delays for AB and CD

AB: 1x + 1x → AB = 5

CD: 3x → CD = 3

An interconnection has a delay quadratic with its length

= 1^2 = 1

= 2^2 = 4

Delay is mainly due to **number of** consecutive **calculations**

Delay is mainly due to **long interconnections**

3. What can we learn from this?

THEN

The netlist should **have** as few calculations as possible! (**This is clear.**)

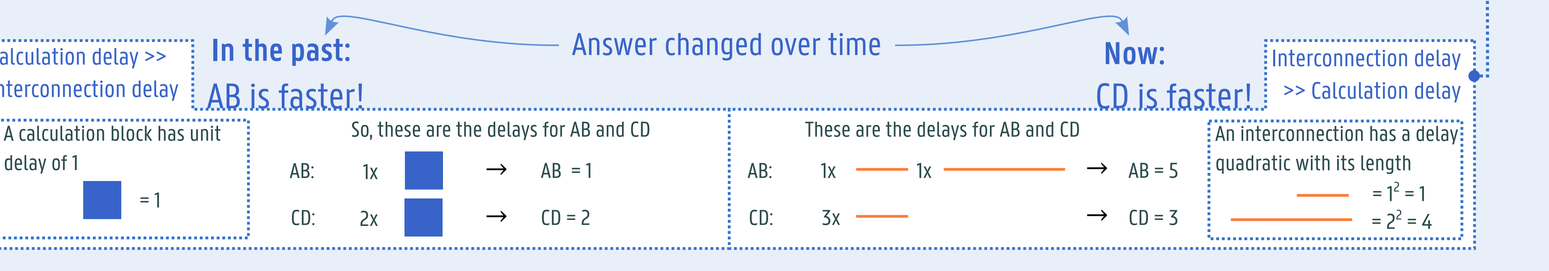
VS

NOW

The netlist should **facilitate** minimizing interconnection length in Placement and Routing! (**Ok, but how?**)

However, the netlist still gets optimized for the first objective instead of the second!

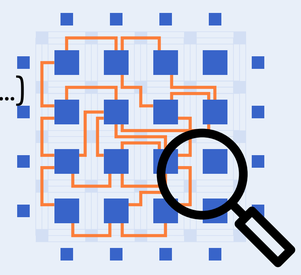
GOAL



PLAN OF ACTION

STEP 1 : Search desirable circuit characteristics: (interconnection complexity, fanout distribution, ...)

STEP 2 : How to transform the netlist to obtain these characteristics?



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